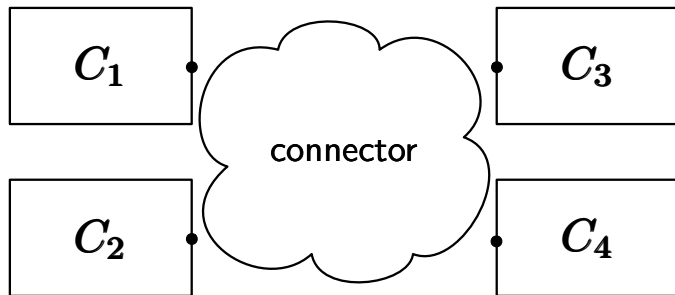


Modeling and Verification of Components and Connectors

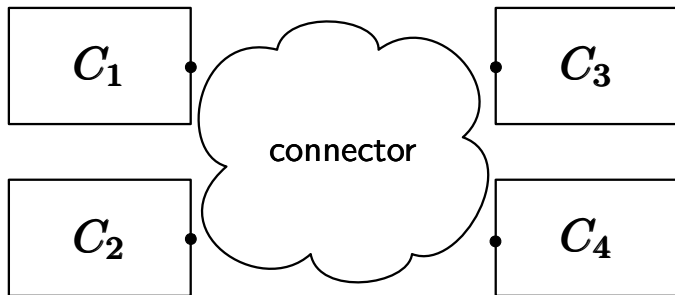
Christel Baier

Technische Universität Dresden

joint work with Tobias Blechmann
Joachim Klein
Sascha Klüppelholz

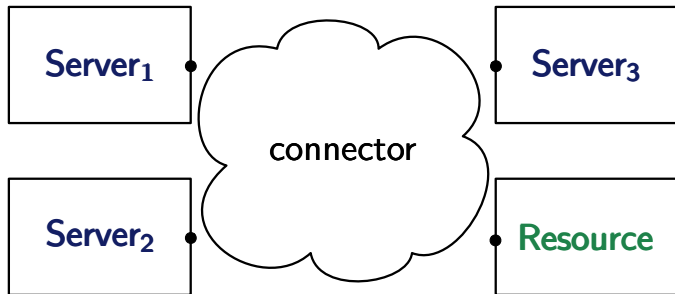


coordination provided by a component connector

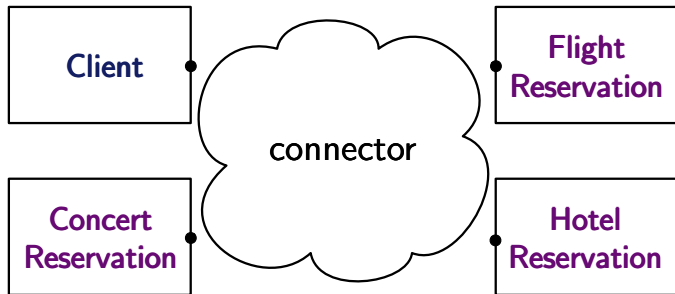


coordination provided by a component connector

- glue code: orchestrates the interactions of possibly heterogeneous components
- synchronous and asynchronous communication, possibly data-dependent

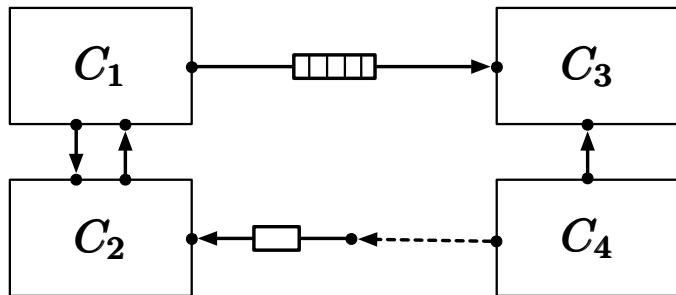


example: connector for orchestrating the interactions of multiple servers and shared resources

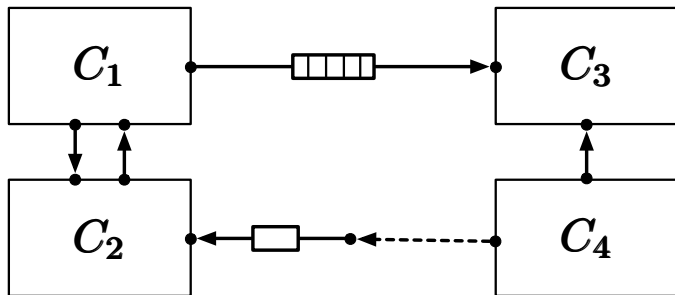


example: orchestrating multiple [webservices](#):

“only book flight and hotel if booking of the concert ticket is successful”

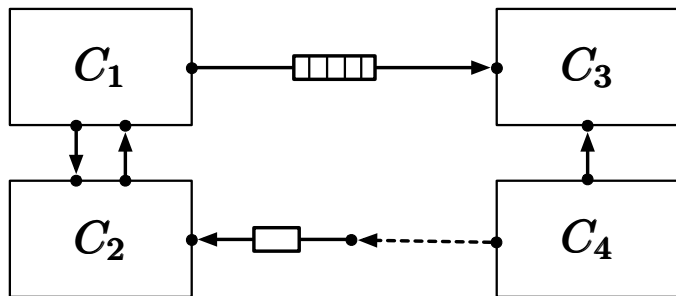


here: **coordination** arises from combination
basic channels forming a **network**



modeling approach for components and connectors, relying on

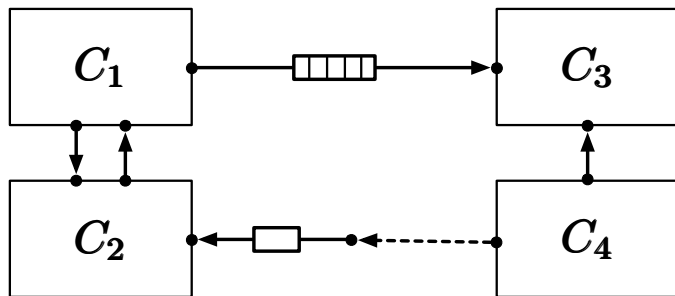
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- operational LTS-like semantics



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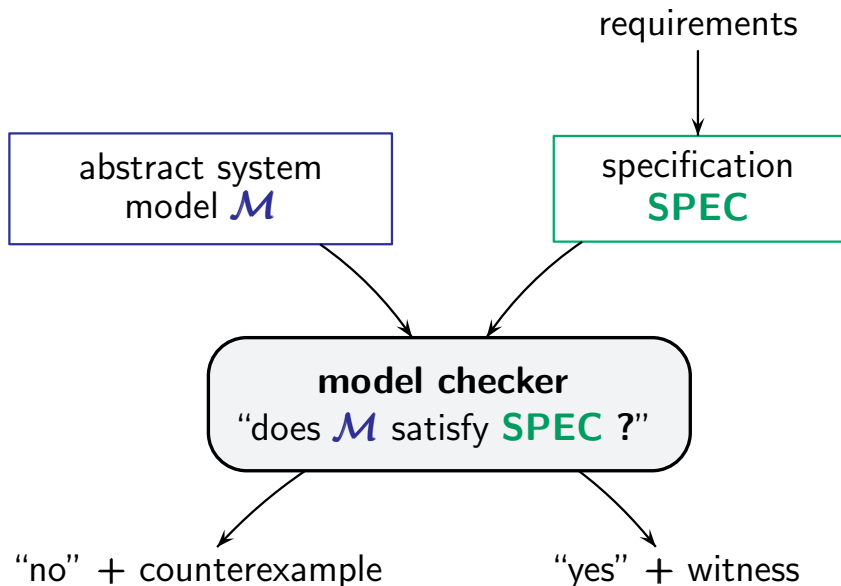


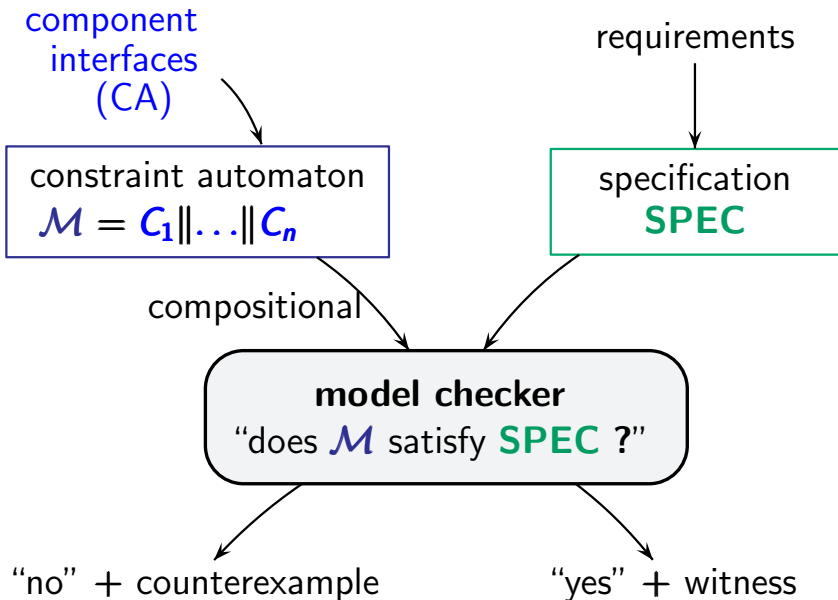
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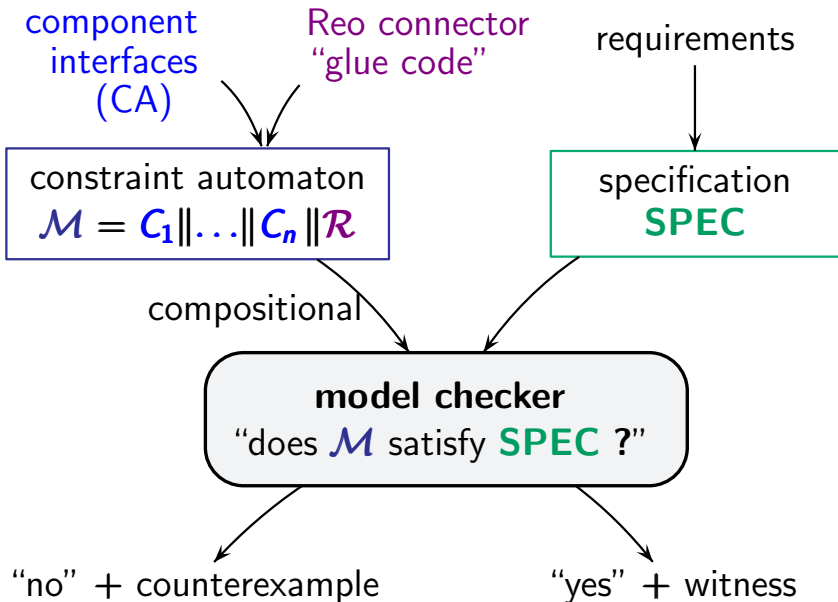
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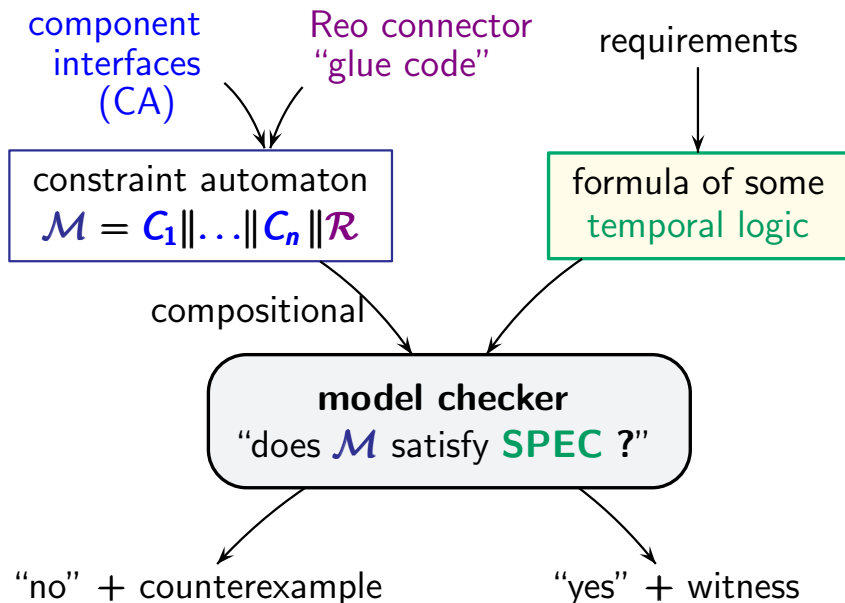
Reo

constraint automata









- 1 Modelling components and connectors
 - constraint automata (CA)
 - coordination language Reo
- 2 Model checking with CA
 - Linear Temporal Logic
 - Alternating Stream Logic
- 3 Synthesis of connectors

1 Modelling components and connectors

constraint automata (CA) ←
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3 Synthesis of connectors

an LTS-like automata model for

- component interfaces C_1, \dots, C_n
- glue code, i.e., Reo network of channels \mathcal{R}
- composite system $C_1 \parallel \dots \parallel C_n \parallel \mathcal{R}$

A constraint automaton is a tuple $\mathcal{A} = (Q, \mathcal{N}, \longrightarrow, Q_0)$

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\mathcal{N}_{in} and \mathcal{N}_{out} are disjoint subsets of \mathcal{N} ,
specifying I/O-ports of a component or connector

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$g \in DC(N)$ data constraint for the data items sent or received at the active ports

Boolean conditions on the sent or received data items at the I/O-ports of components or nodes of the network

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finite, global data domain *Data*

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data values at ports
 A and B agree

finite, global data domain \textit{Data}

sequence of transitions in CA

$$q_0 \xrightarrow{N_1, g_1} q_1 \xrightarrow{N_2, g_2} q_2 \xrightarrow{N_3, g_3} \dots$$

induces a set of executions

$$\eta = q_0 \xrightarrow{c_1} q_1 \xrightarrow{c_2} q_2 \xrightarrow{c_3} \dots$$

where c_1, c_2, c_3, \dots are concurrent I/O operations

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↑
simultaneous
send/receive operations
at the active ports

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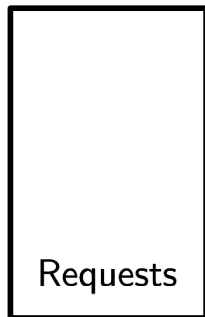
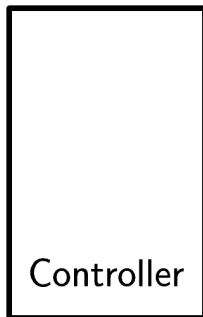
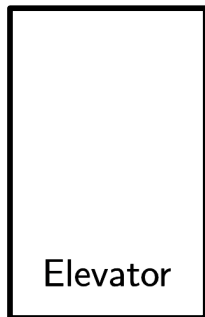
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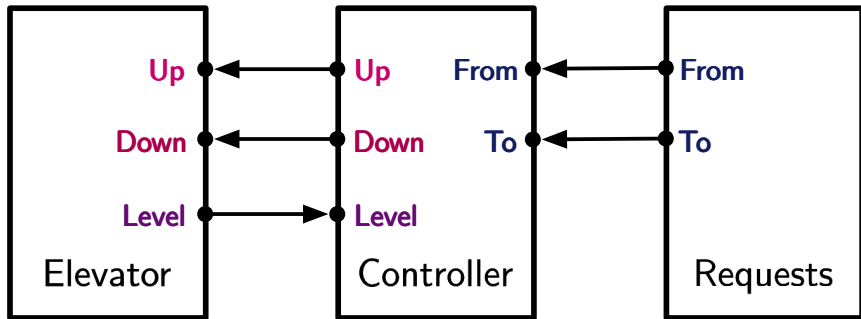
$c_i : N_i \rightarrow \text{Data}$ is a data assignment with $c_i \models g_i$

assigns to each port $A \in N_i$ the data item
sent or received at A



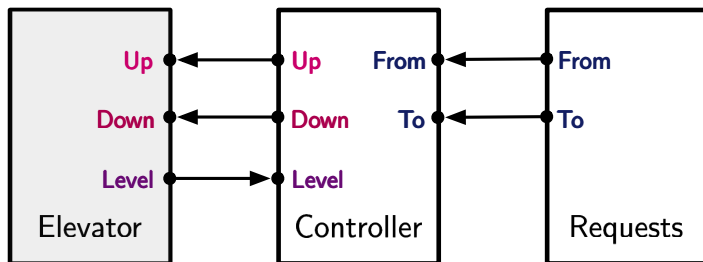
Example: elevator system

250



Example: CA for elevator component

255



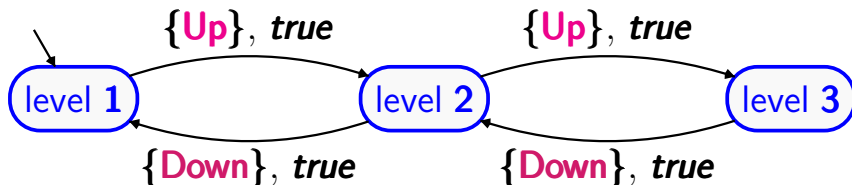
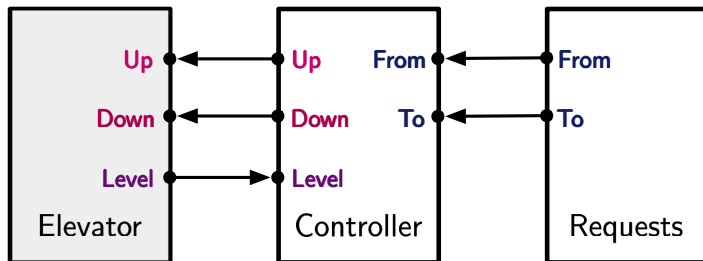
port set $\mathcal{N} = \{\text{Up}, \text{Down}, \text{Level}\}$

$\mathcal{N}_{\text{in}} = \{\text{Up}, \text{Down}\}$, $\mathcal{N}_{\text{out}} = \{\text{Level}\}$

$\text{Data} = \{1, 2, 3\}$ three floors

Example: CA for elevator component

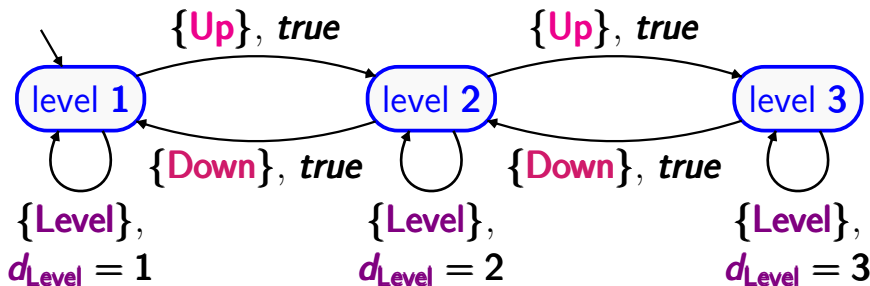
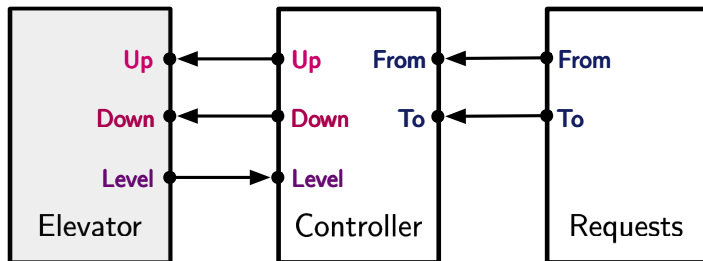
255



Data = {1, 2, 3} three floors

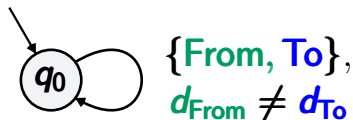
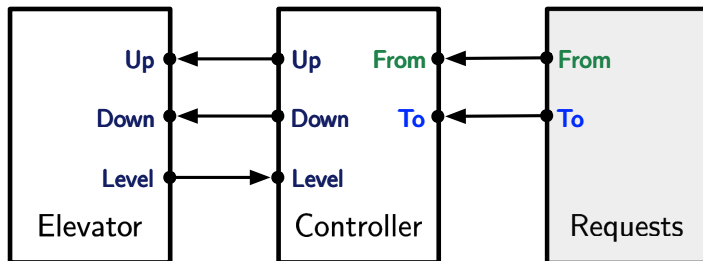
Example: CA for elevator component

255



Example: CA for request component


260



$$\mathcal{N} = \mathcal{N}_{\text{out}} = \{\text{From}, \text{To}\} \quad \mathcal{N}_{\text{in}} = \emptyset$$

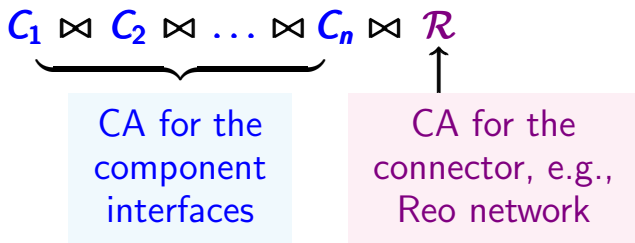
constraint automaton for the **composite system** is built compositionally using parallel operator \bowtie

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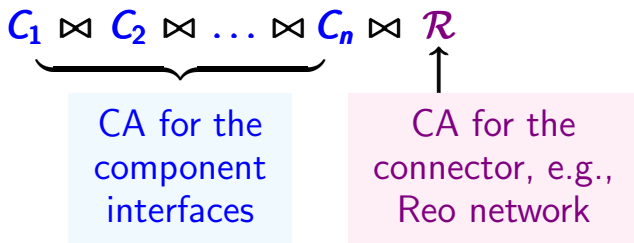
$$C_1 \bowtie C_2 \bowtie \dots \bowtie C_n$$


CA for the
component
interfaces

constraint automaton for the **composite system** is built compositionally using parallel operator \bowtie

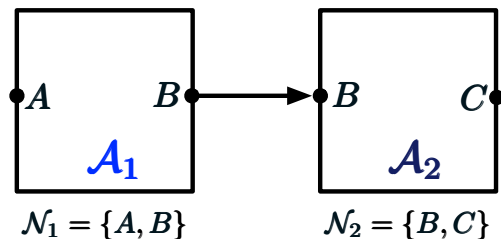


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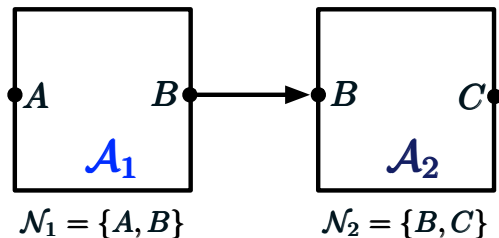


relies on a product construction with

- **synchronization** over shared ports
- **interleaving** of I/O-operations without shared ports

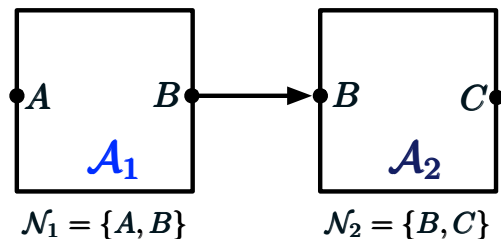


such that classification into input or output ports is “compatible”



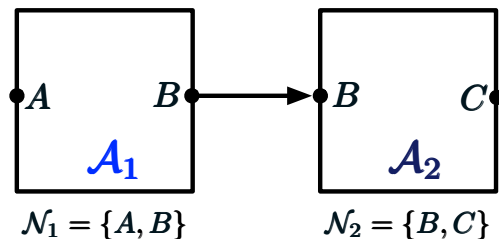
$$\mathcal{A}_1 = (Q_1, \mathcal{N}_1, \longrightarrow_1, Q_0^1) \quad \mathcal{A}_2 = (Q_2, \mathcal{N}_2, \longrightarrow_2, Q_0^2)$$

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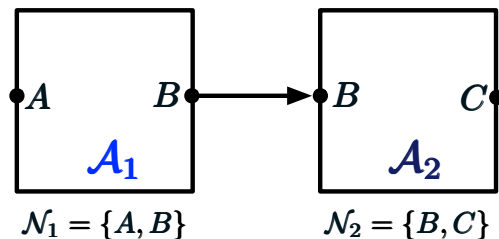
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$$\mathcal{A}_1 \bowtie \mathcal{A}_2 = (Q_1 \times Q_2, \dots)$$



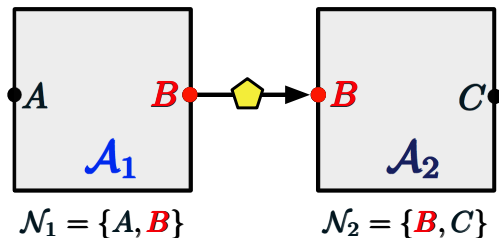
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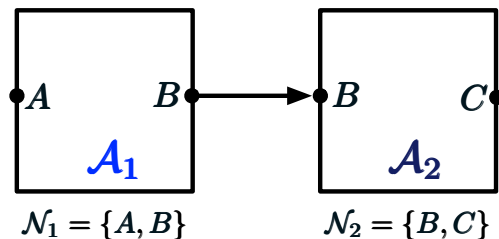
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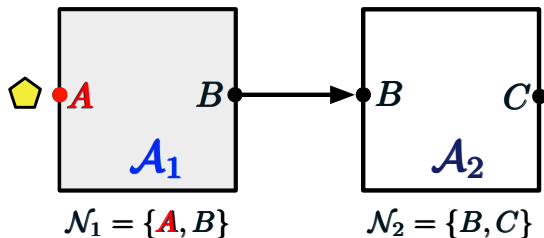
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synchronizing over the shared ports
 $B \in \mathcal{N}_1 \cap \mathcal{N}_2$



I/O-operations of \mathcal{A}_1 without shared ports

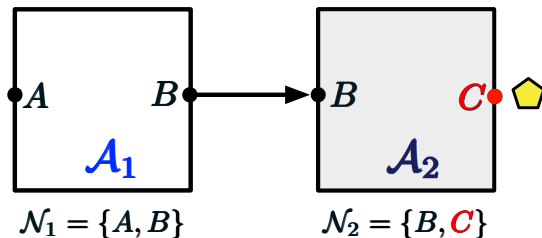
$$\frac{q_1 \xrightarrow{N_1, g_1} q'_1 \text{ and } N_1 \cap \mathcal{N}_2 = \emptyset}{\langle q_1, q_2 \rangle \xrightarrow{N_1, g_1} \langle q'_1, q_2 \rangle}$$



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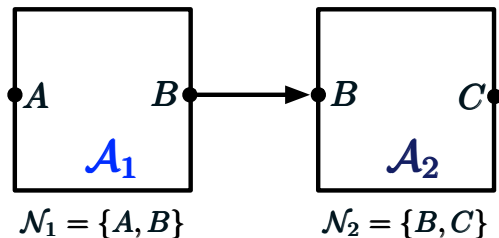
“data flow only at non-shared ports of \mathcal{A}_1 ”



I/O-operations of \mathcal{A}_2 without shared ports

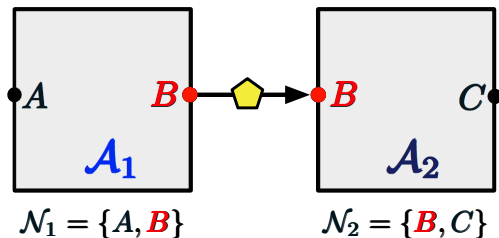
$$\frac{q_2 \xrightarrow{N_2, g_2} q'_2 \text{ and } N_2 \cap \mathcal{N}_1 = \emptyset}{\langle q_1, q_2 \rangle \xrightarrow{N_2, g_2} \langle q_1, q'_2 \rangle}$$

“data flow only at non-shared ports of \mathcal{A}_2 ”



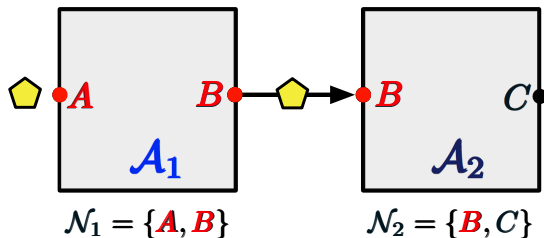
synchronized data flow at shared ports:

$$\frac{q_1 \xrightarrow{N_1, g_1} q'_1 \wedge q_2 \xrightarrow{N_2, g_2} q'_2 \wedge N_1 \cap \mathcal{N}_2 = N_2 \cap \mathcal{N}_1}{\langle q_1, q_2 \rangle \xrightarrow{N_1 \cup N_2, g_1 \wedge g_2} \langle q'_1, q'_2 \rangle}$$



synchronized data flow at shared ports:

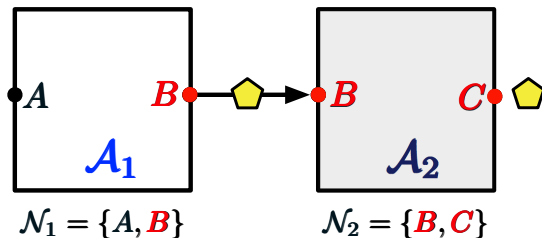
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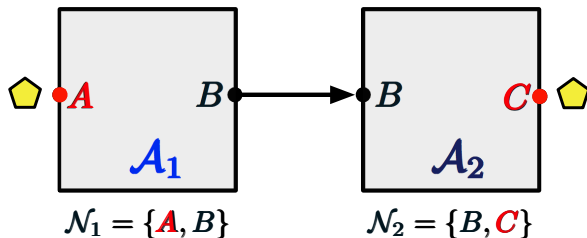
possibly in parallel with data flow at non-shared ports



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 \end{array}$$

... covers the case where $N_1 \cap \mathcal{N}_2 = N_2 \cap \mathcal{N}_1 = \emptyset$
 (needed to ensure associativity)

1 Modelling components and connectors

constraint automata (CA)

coordination language Reo ←

2 Model checking with CA

Linear Temporal Logic

Alternating Stream Logic

3 Synthesis of connectors

- exogenous coordination aims to provide a strict separation between **computation** and **coordination**

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Reo network: graph of channels

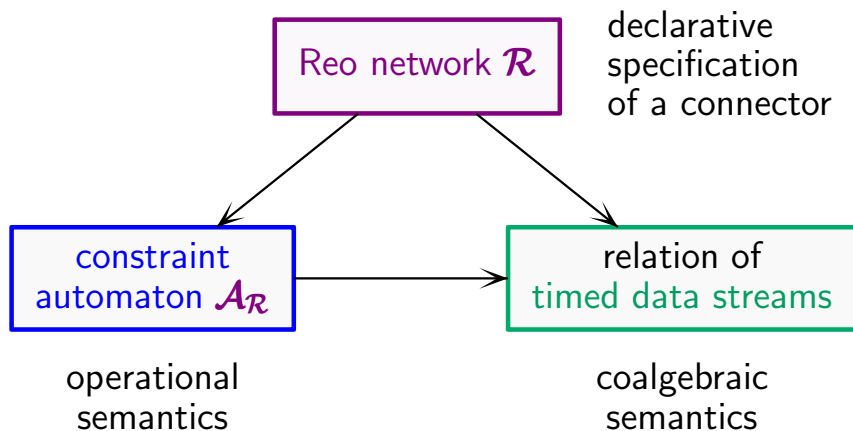
edges: channels

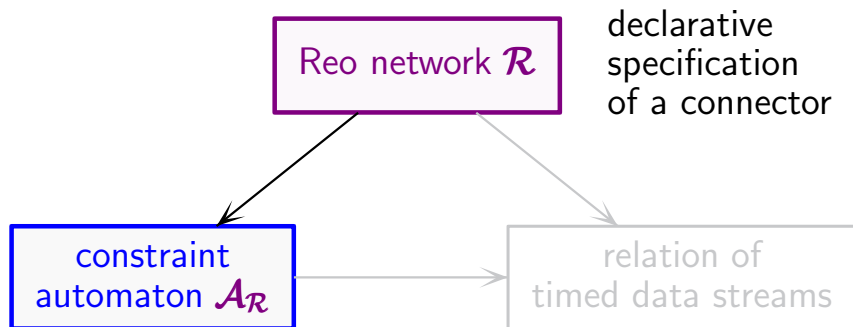
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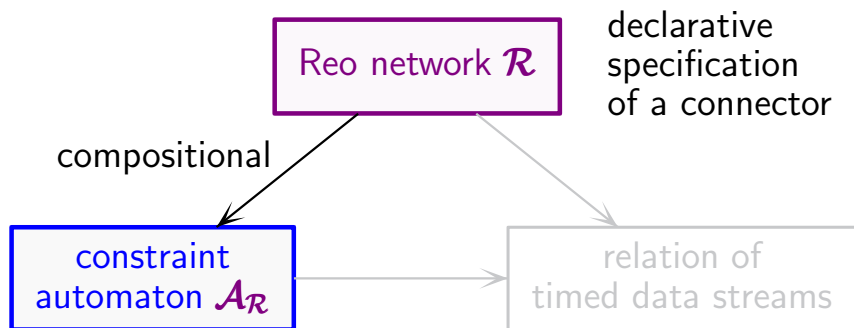
Reo network: graph of channels
edges: channels
nodes: combine several channel ends

← semantics:
**constraint
automaton**



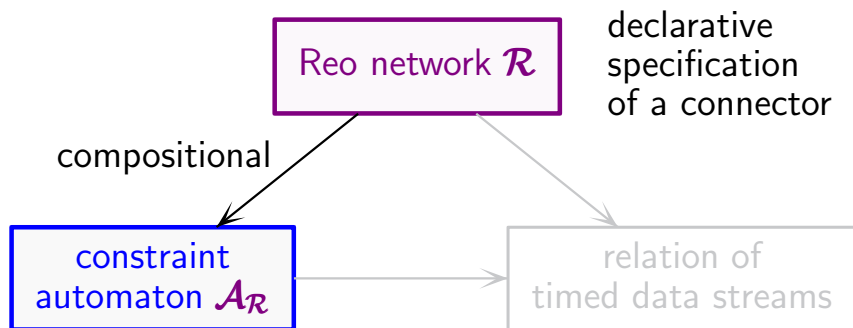


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(e.g., content of FIFO channels)



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composite system: $\mathcal{C}_1 \bowtie \dots \bowtie \mathcal{C}_n \bowtie \mathcal{A}_{\mathcal{R}}$

1 Modelling components and connectors

constraint automata (CA)

coordination language Reo

Reo channels



Reo nodes

2 Model checking with CA

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data item leaves channel

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- have **two channel ends**, each can be either a source or a sink end

- * **source end**:

data item enters channel





input port

- * **sink end**:

data item leaves channel




output port

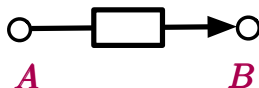
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 - * **source end**:
data item enters channel ← 
 - * **sink end**:
data item leaves channel ← 
- from library of **basic channels** or user defined (CA + types of channel end)

- FIFO channel
- synchronous channel
- synchronous drain
- synchronous spout
- filter channel
- non-deterministic lossy channel

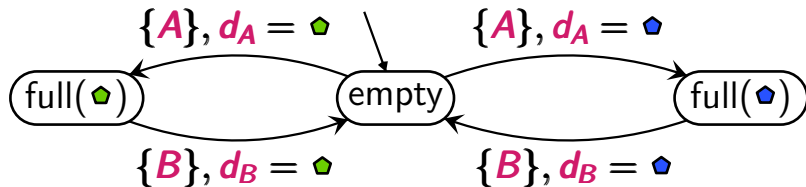
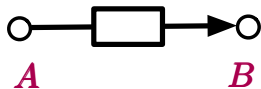
- FIFO channel
- synchronous channel
- synchronous drain
- synchronous spout
- filter channel
- non-deterministic lossy channel



asynchronous
communication
via buffer



$$\mathcal{N}_{\text{in}} = \{A\} \quad \mathcal{N}_{\text{out}} = \{B\}$$

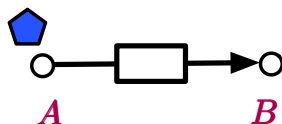


$$\mathcal{N}_{\text{in}} = \{A\}$$

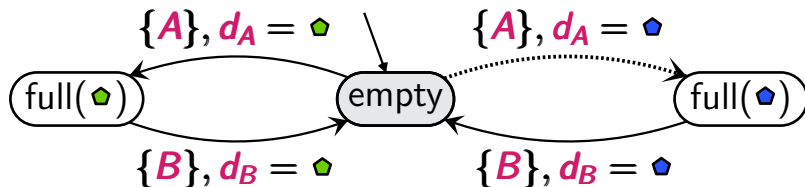
$$\mathcal{N}_{\text{out}} = \{B\}$$

FIFO channel with 1 buffer cell

310



	A	B
t_1		

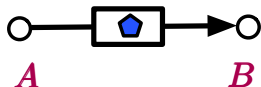


$$\mathcal{N}_{\text{in}} = \{A\}$$

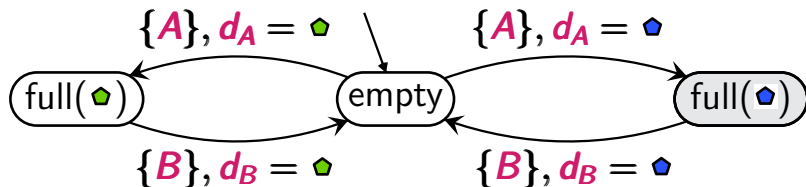
$$\mathcal{N}_{\text{out}} = \{B\}$$

FIFO channel with 1 buffer cell

310



	A	B
t_1		

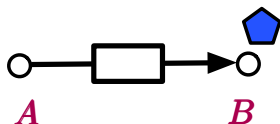


$$\mathcal{N}_{\text{in}} = \{A\}$$

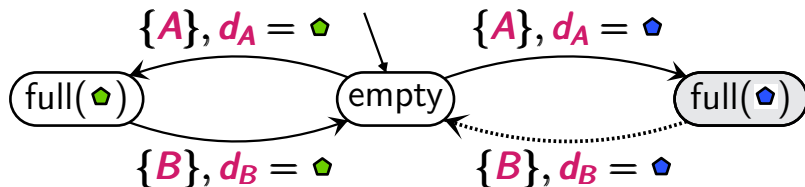
$$\mathcal{N}_{\text{out}} = \{B\}$$

FIFO channel with 1 buffer cell

310



	A	B
t_1		
t_2		

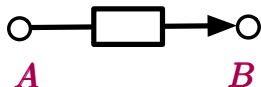




$$\mathcal{N}_{\text{in}} = \{A\}$$

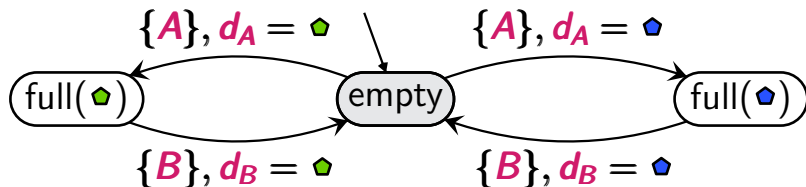
$$\mathcal{N}_{\text{out}} = \{B\}$$

FIFO channel with 1 buffer cell

310



	A	B
t_1		
t_2		

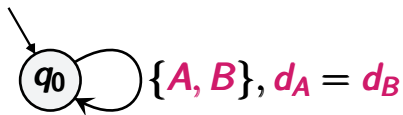
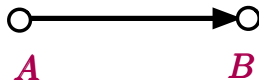


$$\mathcal{N}_{\text{in}} = \{A\}$$

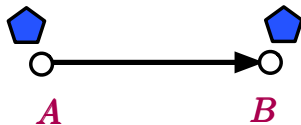
$$\mathcal{N}_{\text{out}} = \{B\}$$



- FIFO channel
- **synchronous channel**
- synchronous drain
- synchronous spout
- filter channel
- non-deterministic lossy channel

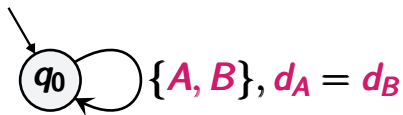




$$\mathcal{N}_{\text{in}} = \{A\} \quad \mathcal{N}_{\text{out}} = \{B\}$$

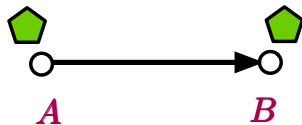


	A	B
t_1		

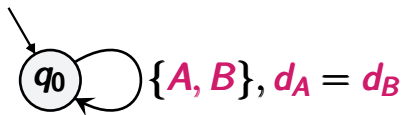


$$\mathcal{N}_{\text{in}} = \{A\}$$

$$\mathcal{N}_{\text{out}} = \{B\}$$

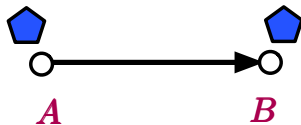


	<i>A</i>	<i>B</i>
t_1	blue pentagon	blue pentagon
t_2	green pentagon	green pentagon

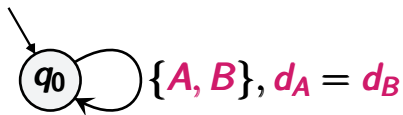


$$\mathcal{N}_{\text{in}} = \{A\}$$

$$\mathcal{N}_{\text{out}} = \{B\}$$



	<i>A</i>	<i>B</i>
t_1		
t_2		
t_3		

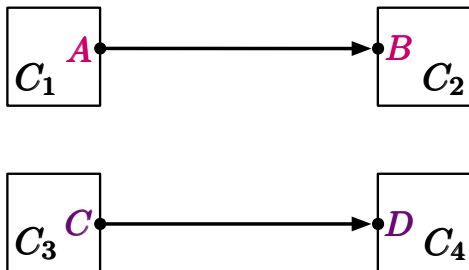


$$\mathcal{N}_{\text{in}} = \{A\}$$

$$\mathcal{N}_{\text{out}} = \{B\}$$

Example: Reo network and four components

450

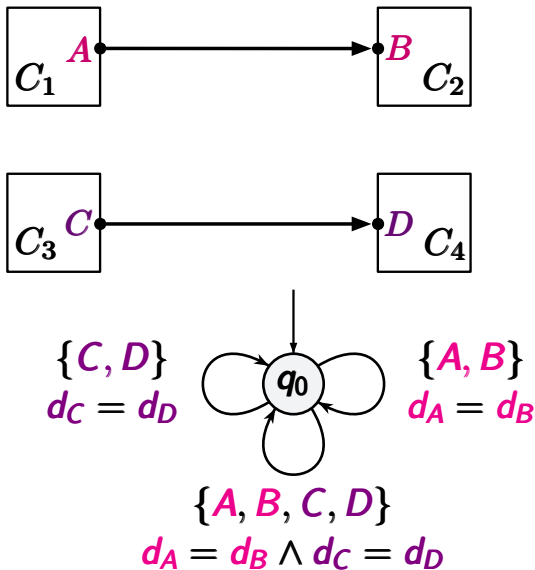


Reo network with two channels:

- synchronous channel AB connecting components C_1 with C_2
- synchronous channel CD connecting components C_3 with C_4

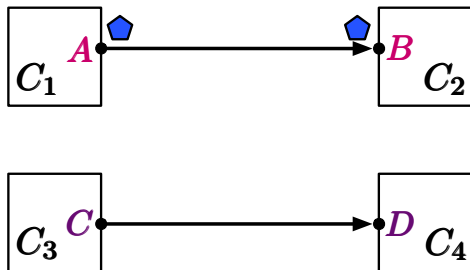
Example: Reo network and four components

450

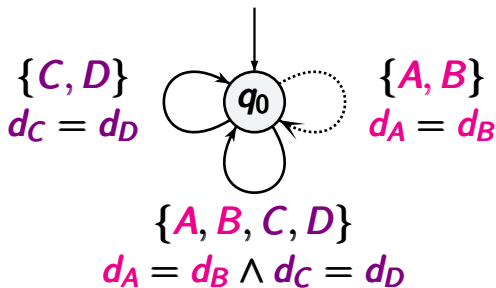


Example: Reo network and four components

450

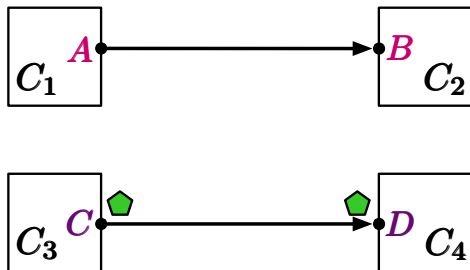


	A	B	C	D
t_1	blue pentagon	blue pentagon		

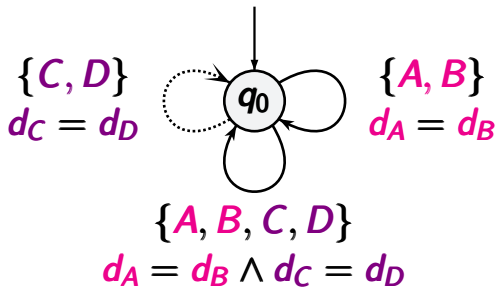


Example: Reo network and four components

450

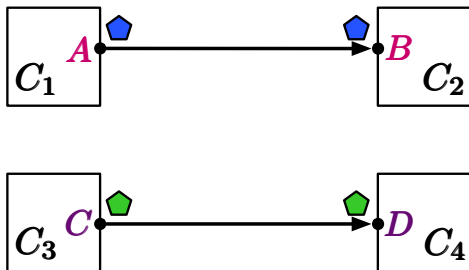


	A	B	C	D
t_1				
t_2				

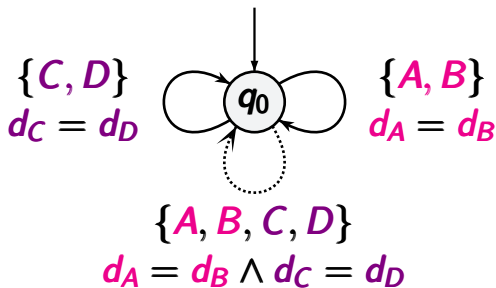


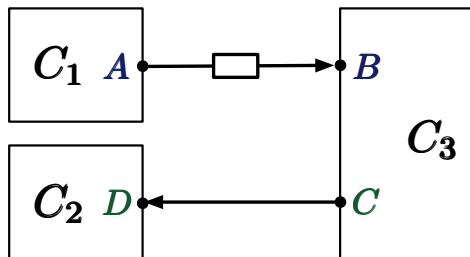
Example: Reo network and four components

450



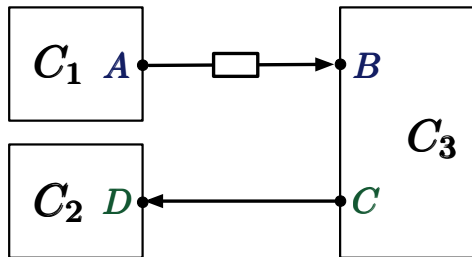
	<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>
t_1	blue pentagon	blue pentagon		
t_2			green pentagon	green pentagon
t_3	blue pentagon	blue pentagon	green pentagon	green pentagon



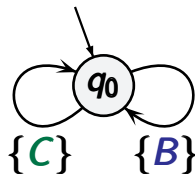


system with three components

- fifo channel AB
- synchronous channel CD



component
interface for C_3



system with three components

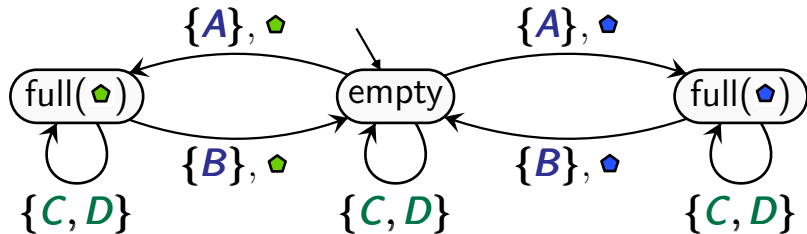
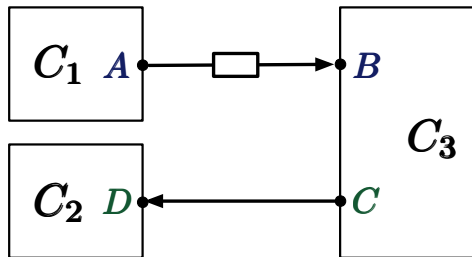
- fifo channel AB
- synchronous channel CD

$$\mathcal{N}_{\text{in}} = \{B\}$$

$$\mathcal{N}_{\text{out}} = \{C\}$$

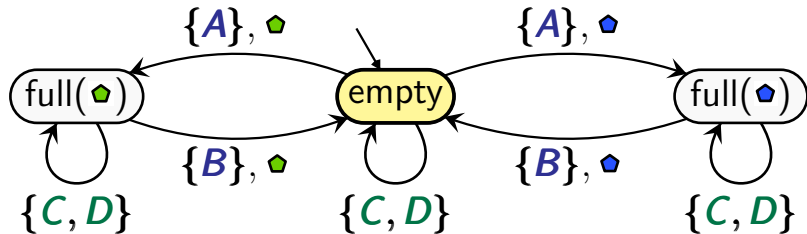
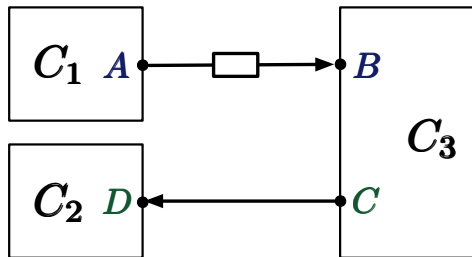
Example: network and its CA-semantics

150



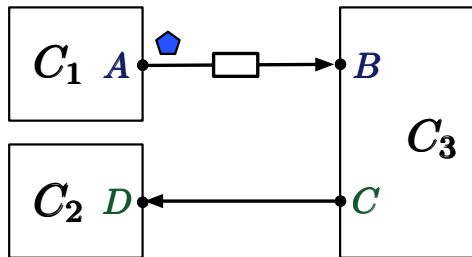
Example: network and its CA-semantics

150

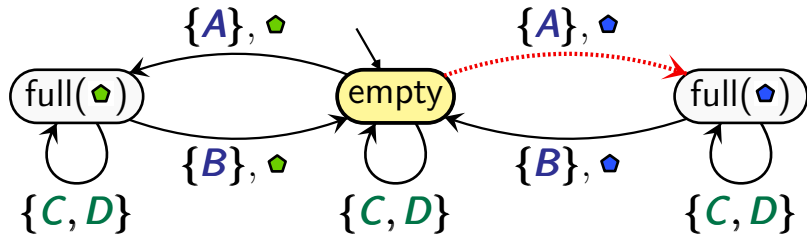


Example: network and its CA-semantics

150

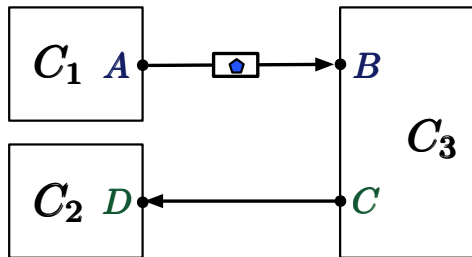


	A	B	C	D
t_1	blue pentagon			

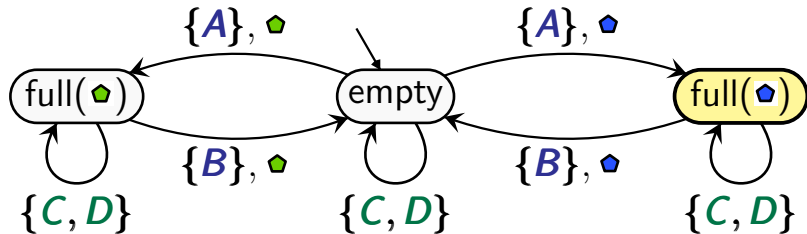


Example: network and its CA-semantics

150

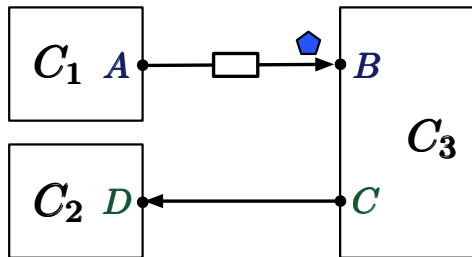


	A	B	C	D
t_1	blue pentagon			

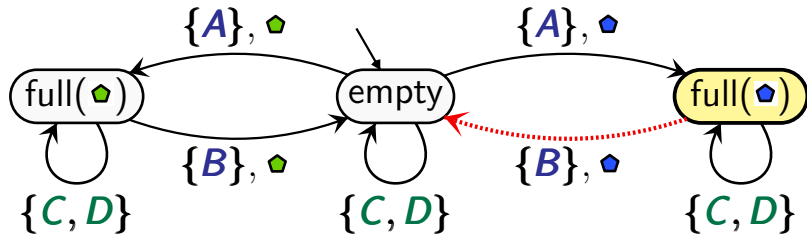


Example: network and its CA-semantics

150

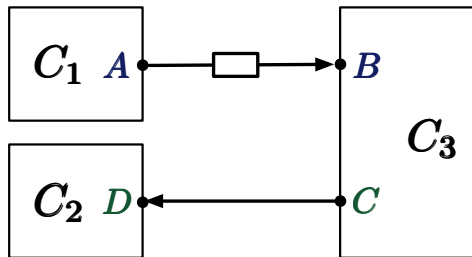


	A	B	C	D
t_1	blue pentagon			
t_2		blue pentagon		

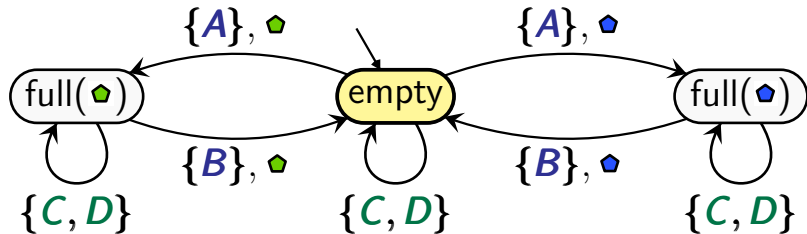


Example: network and its CA-semantics

150

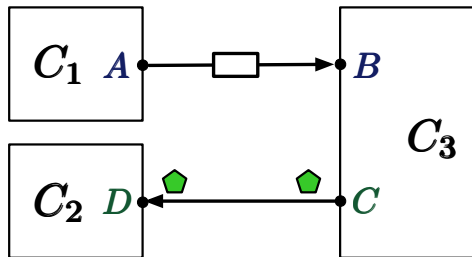


	A	B	C	D
t_1				
t_2				

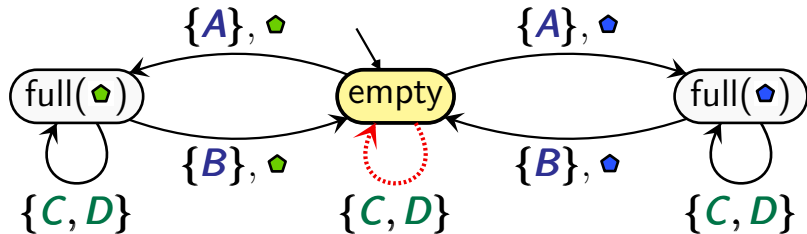


Example: network and its CA-semantics

150

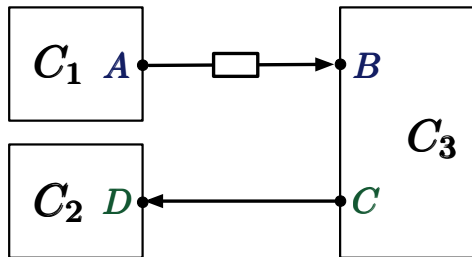


	A	B	C	D
t_1				
t_2				
t_3				

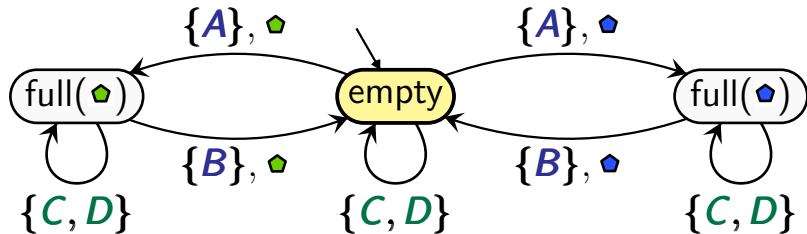


Example: network and its CA-semantics

150

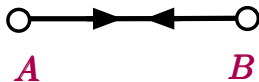


	A	B	C	D
t_1				
t_2				
t_3				

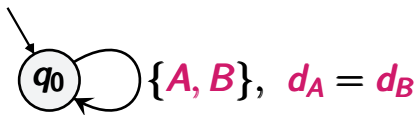


- FIFO channel
- synchronous channel
- synchronous drain
- synchronous spout
- filter channel
- non-deterministic lossy channel

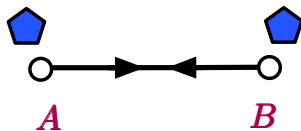
variants of
synchronous
channels



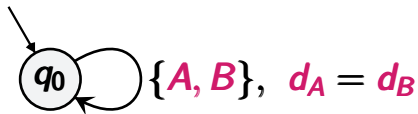
two source ends
(input ports)



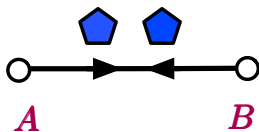
$$\mathcal{N}_{\text{in}} = \{A, B\} \quad \mathcal{N}_{\text{out}} = \emptyset$$





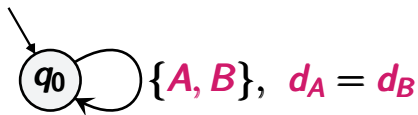
	A	B
t_1		



$$\mathcal{N}_{\text{in}} = \{A, B\} \quad \mathcal{N}_{\text{out}} = \emptyset$$



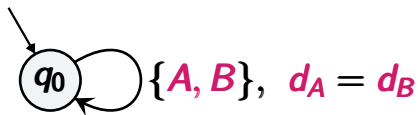
	A	B
t_1		



$$\mathcal{N}_{\text{in}} = \{A, B\} \quad \mathcal{N}_{\text{out}} = \emptyset$$



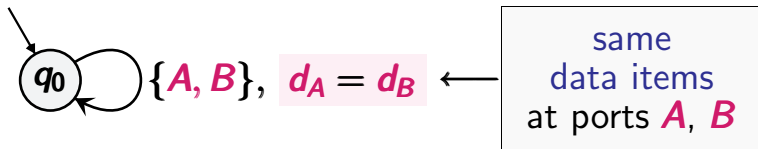
	A	B
t_1		



$$\mathcal{N}_{\text{in}} = \{A, B\} \quad \mathcal{N}_{\text{out}} = \emptyset$$



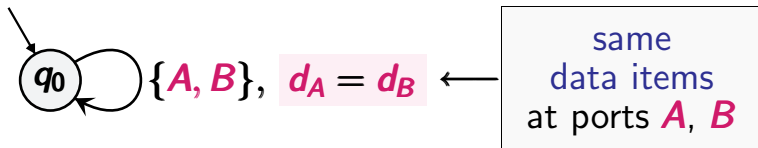
	A	B
t_1	blue pentagon	blue pentagon
t_2	green pentagon	green pentagon



$$\mathcal{N}_{\text{in}} = \{A, B\} \quad \mathcal{N}_{\text{out}} = \emptyset$$



	A	B
t_1	blue pentagon	blue pentagon
t_2	green pentagon	green pentagon
t_3	red pentagon	red pentagon



$$\mathcal{N}_{\text{in}} = \{A, B\} \quad \mathcal{N}_{\text{out}} = \emptyset$$



	A	B
t_1	red pentagon	blue pentagon
t_2	green pentagon	blue pentagon
t_3	blue pentagon	green pentagon

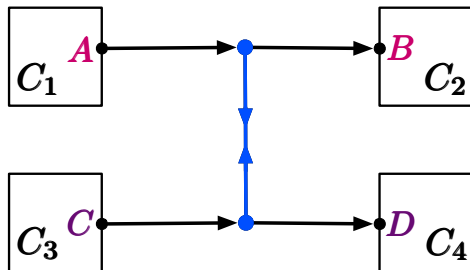


arbitrary
data items
at ports A, B

$$\mathcal{N}_{\text{in}} = \{A, B\} \quad \mathcal{N}_{\text{out}} = \emptyset$$

Example: Reo network with synchronous drain

460

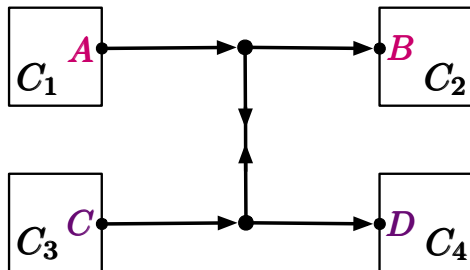


Reo network with four components

- synchronous data flow from A to B
- synchronous data flow from C to D
- **synchronous drain** ensures synchronization of all four components

Example: Reo network with synchronous drain

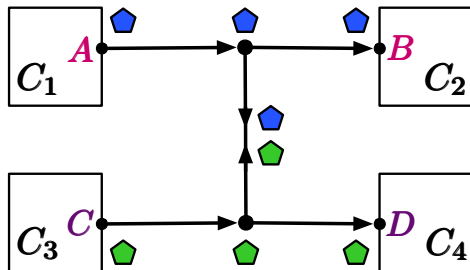
460

 $\{A, B, C, D\}$

$$d_A = d_B \wedge d_C = d_D$$

Example: Reo network with synchronous drain

460



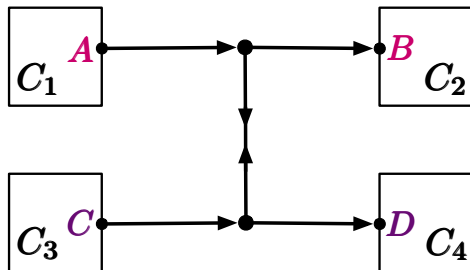
	<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>
t_1				

 $\{A, B, C, D\}$

$$d_A = d_B \wedge d_C = d_D$$

Example: Reo network with synchronous drain

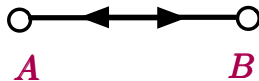
460



	<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>
t_1				
t_2				
t_3				

 $\{A, B, C, D\}$

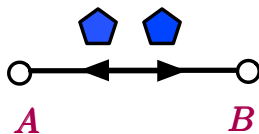
$$d_A = d_B \wedge d_C = d_D$$





two sink ends
(output ports)



$$\mathcal{N}_{\text{in}} = \emptyset \quad \mathcal{N}_{\text{out}} = \{A, B\}$$

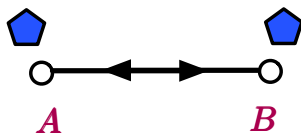




	A	B
t_1		



$$\mathcal{N}_{\text{in}} = \emptyset$$

$$\mathcal{N}_{\text{out}} = \{A, B\}$$

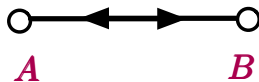






	A	B
t_1		



$$\mathcal{N}_{\text{in}} = \emptyset$$

$$\mathcal{N}_{\text{out}} = \{A, B\}$$









	A	B
t_1		
t_2		



$$\mathcal{N}_{\text{in}} = \emptyset$$

$$\mathcal{N}_{\text{out}} = \{A, B\}$$



	A	B
t_1		
t_2		
t_3		

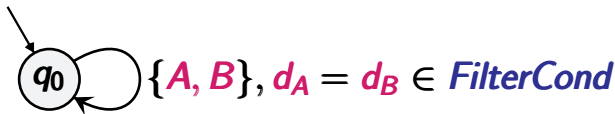


$$\mathcal{N}_{\text{in}} = \emptyset$$

$$\mathcal{N}_{\text{out}} = \{A, B\}$$



“ordinary”
synchronous channel
with filter condition

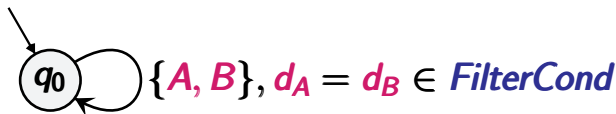


$$\mathcal{N}_{\text{in}} = \{A\} \quad \mathcal{N}_{\text{out}} = \{B\}$$



	<i>A</i>	<i>B</i>
t_1	blue pentagon	blue pentagon
t_2	green pentagon	green pentagon
t_3	blue pentagon	blue pentagon

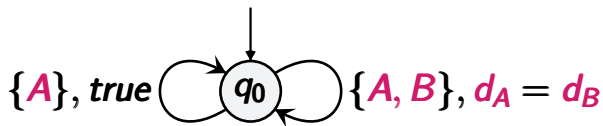
blue pentagon, green pentagon \in *FilterCond*



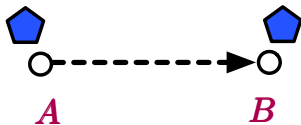
$$\mathcal{N}_{\text{in}} = \{A\} \quad \mathcal{N}_{\text{out}} = \{B\}$$





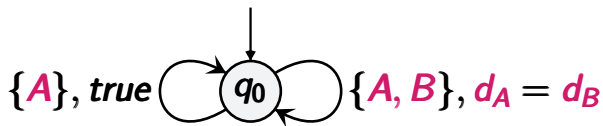
synchronous channel
where written data items
can be lost



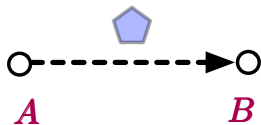
$$\mathcal{N}_{\text{in}} = \{A\} \quad \mathcal{N}_{\text{out}} = \{B\}$$






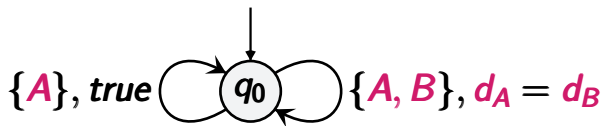
	<i>A</i>	<i>B</i>
t_1		



$$\mathcal{N}_{\text{in}} = \{A\} \quad \mathcal{N}_{\text{out}} = \{B\}$$



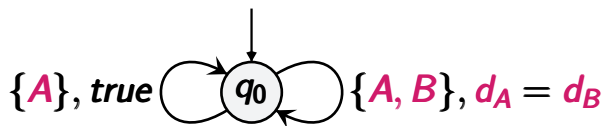
	A	B
t_1		
t_2		



$$\mathcal{N}_{\text{in}} = \{A\} \quad \mathcal{N}_{\text{out}} = \{B\}$$



	A	B
t_1	blue pentagon	blue pentagon
t_2	blue pentagon	
t_3	green pentagon	



$$\mathcal{N}_{\text{in}} = \{A\} \quad \mathcal{N}_{\text{out}} = \{B\}$$

1 Modelling components and connectors

constraint automata (CA)

coordination language Reo

Reo channels

Reo nodes



2 Model checking with CA

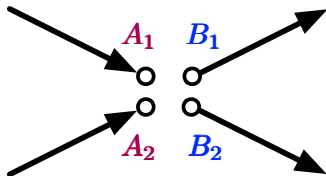
Linear Temporal Logic

Alternating Stream Logic

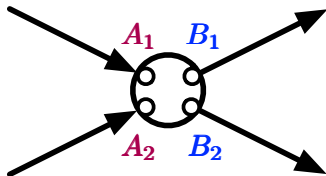
3 Synthesis of connectors

- arise when channel ends are joined
- coordinate the coincident sink and source ends

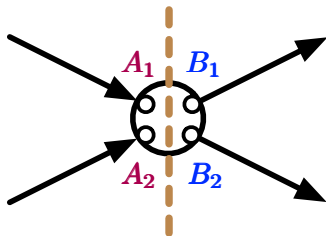
- arise when channel ends are joined
- coordinate the coincident sink and source ends



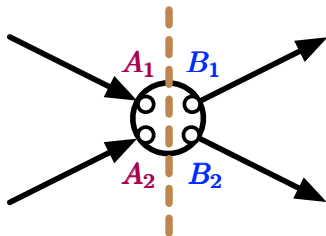
- arise when channel ends are joined
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- arise when channel ends are joined
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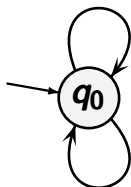
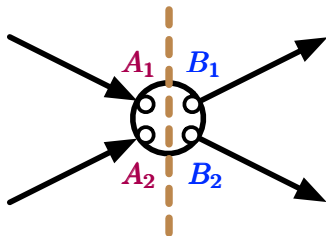
- arise when channel ends are joined
- coordinate the coincident sink and source ends



nondeterministic merge
for receive operations
at the **sink ends**

synchronous
send operation
at the **source ends**

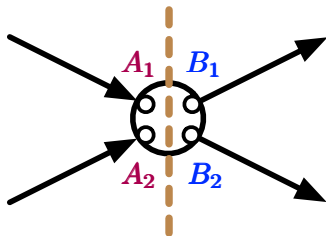
- arise when channel ends are joined
- coordinate the coincident sink and source ends



$$\{A_1, B_1, B_2\}, \quad d_{A_1} = d_{B_1} = d_{B_2}$$

$$\{A_2, B_1, B_2\}, \quad d_{A_2} = d_{B_1} = d_{B_2}$$

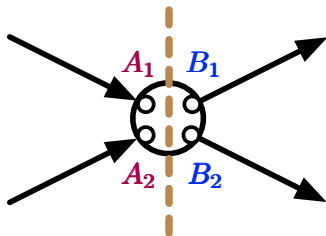
- arise when channel ends are joined
- coordinate the coincident sink and source ends



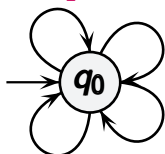
nondeterministic merge
for receive operations
at the **sink ends**

nondeterministic choice
for the send operations
at the **source ends**

- arise when channel ends are joined
- coordinate the coincident sink and source ends



$$\{A_1, B_1\}, d_{A_1} = d_{B_1}$$



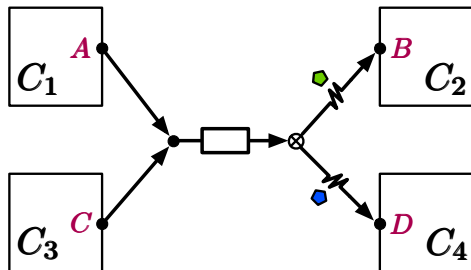
$$\{A_1, B_2\}, d_{A_1} = d_{B_2}$$

$$\{A_2, B_1\}, d_{A_2} = d_{B_1}$$

$$\{A_2, B_2\}, d_B = d_{B_2}$$

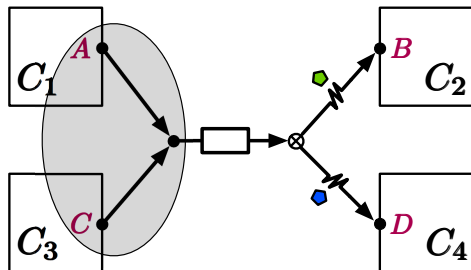
Example: Reo network with buffering & filtering

470

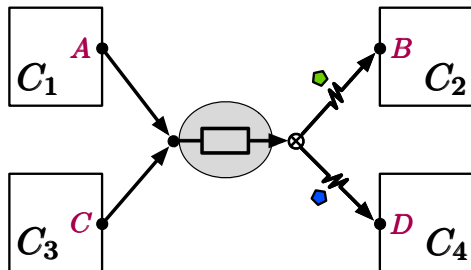


Example: Reo network with buffering & filtering

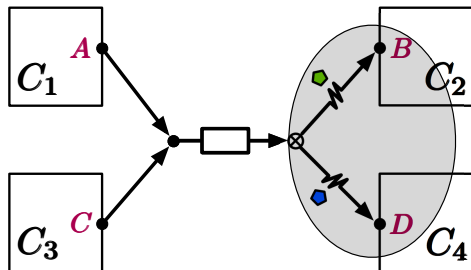
470



- nondeterministic merge between A and C ...



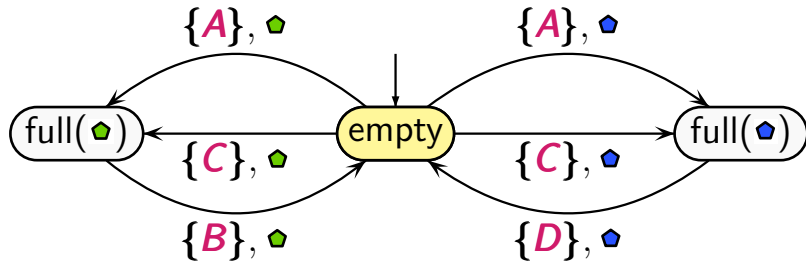
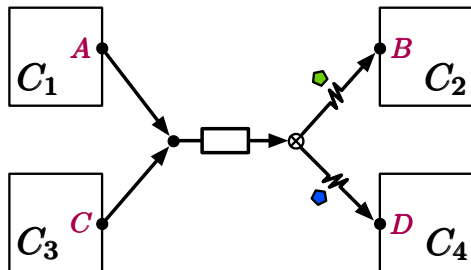
- nondeterministic merge between A and C ...
- data item d written at A or C is stored in the buffer



- nondeterministic merge between A and C ...
- data item d written at A or C is stored in the buffer
if d is green then it will be routed to B
if d is blue then it will be routed to D

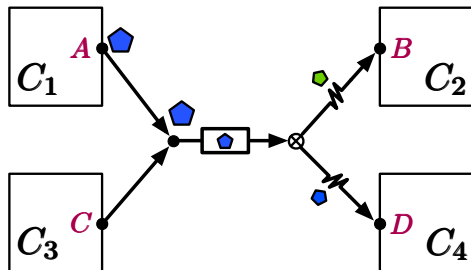
Example: Reo network with buffering & filtering

470

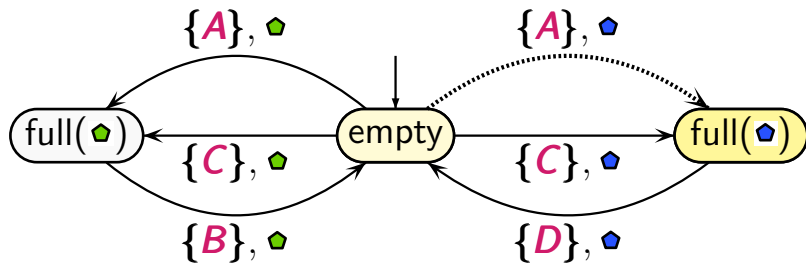


Example: Reo network with buffering & filtering

470

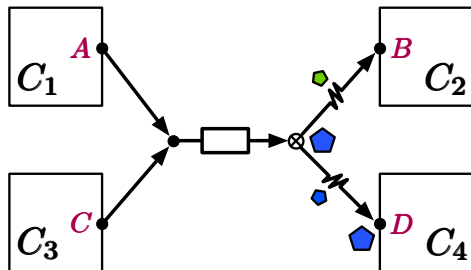


	A	B	C	D
t_1				

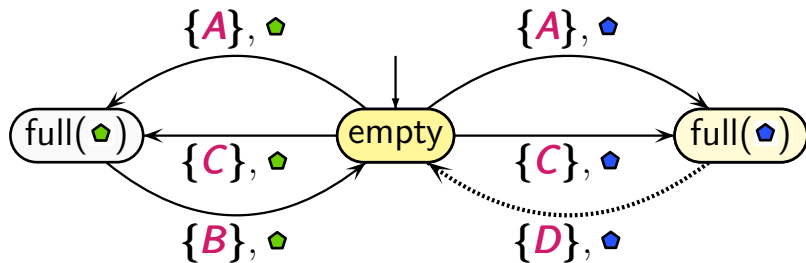


Example: Reo network with buffering & filtering

470

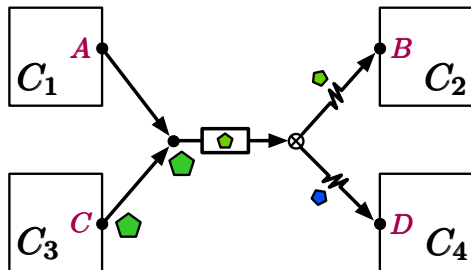


	A	B	C	D
t_1				
t_2				

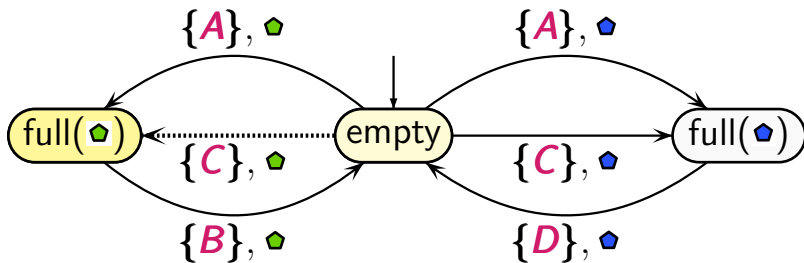


Example: Reo network with buffering & filtering

470

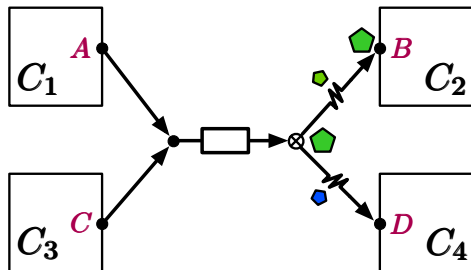


	A	B	C	D
t_1				
t_2				
t_3				

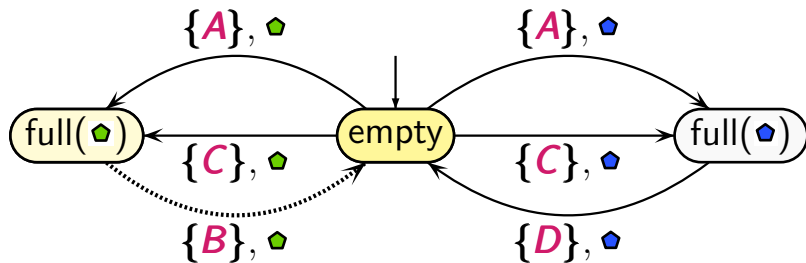


Example: Reo network with buffering & filtering

470

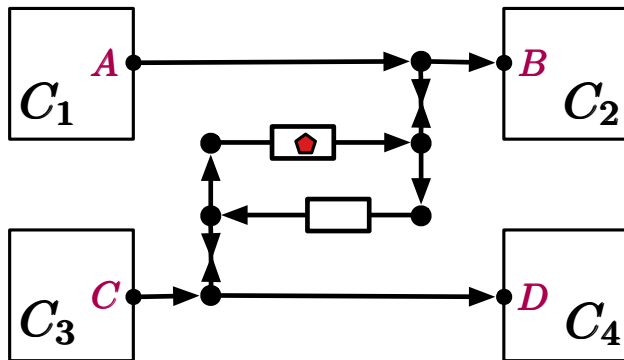


	A	B	C	D
t_1				
t_2				
t_3				
t_4				



Example: Reo network for a sequencer

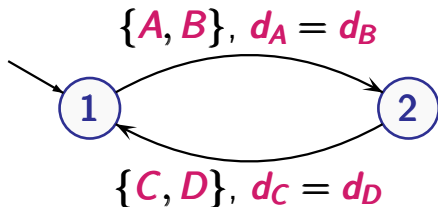
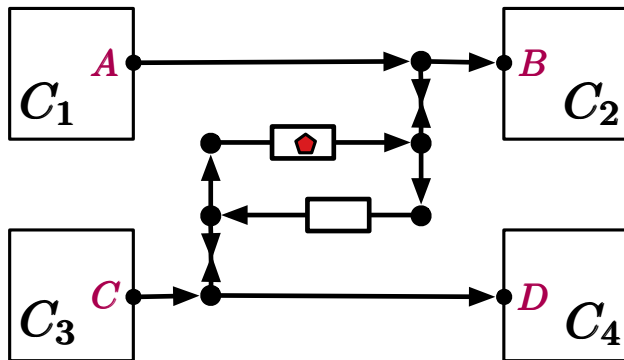
480



alternating data flow between C_1 and C_2 via AB
and between C_3 and C_4 via CD

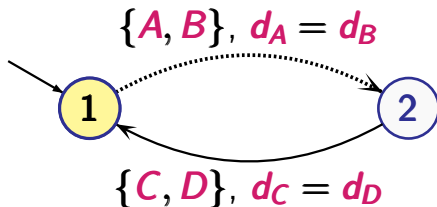
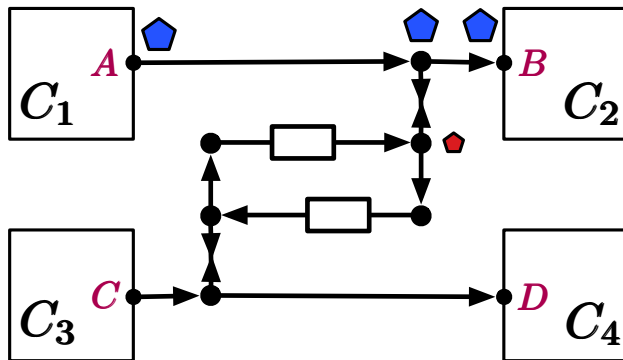
Example: Reo network for a sequencer

480



Example: Reo network for a sequencer

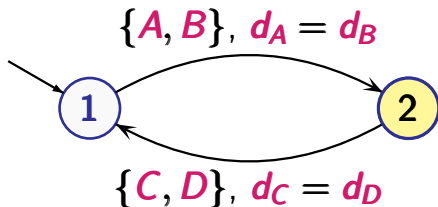
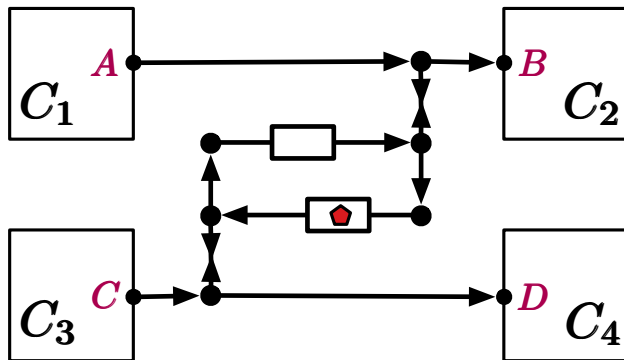
480



	A	B	C	D
t_1	blue pentagon	blue pentagon		

Example: Reo network for a sequencer

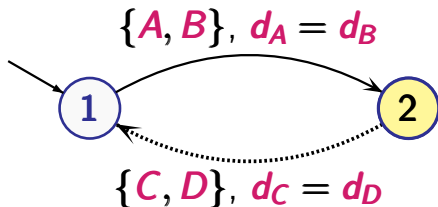
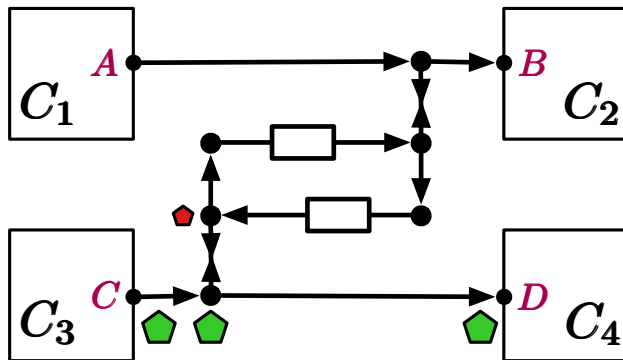
480



	<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>
t_1	⬠	⬠		

Example: Reo network for a sequencer

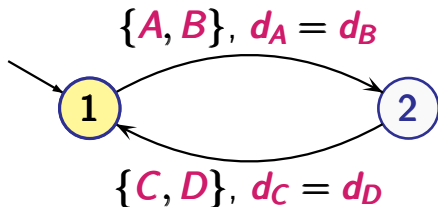
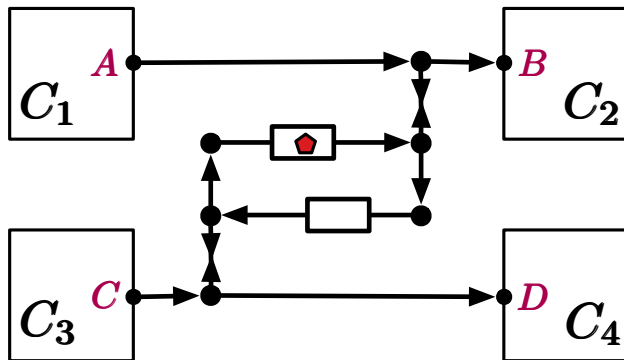
480



	A	B	C	D
t_1				
t_2				

Example: Reo network for a sequencer

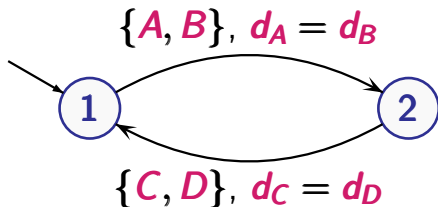
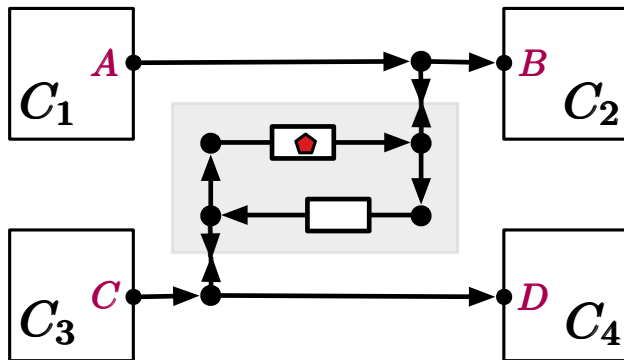
480



	<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>
t_1				
t_2				

Example: Reo network for a sequencer

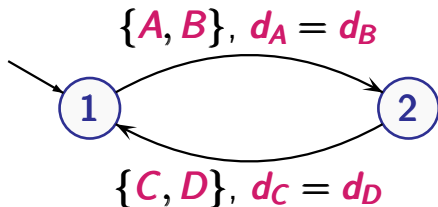
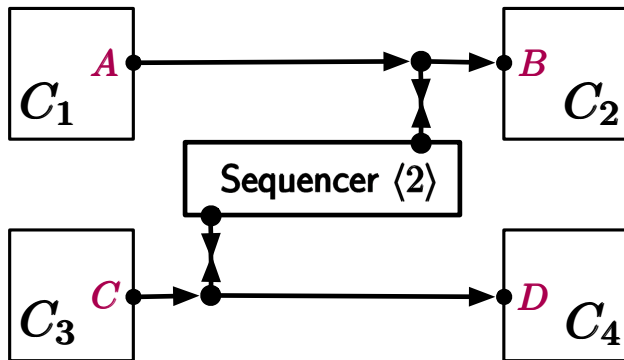
480



	<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>
t_1				
t_2				

Example: Reo network for a sequencer

480



	A	B	C	D
t_1	■	■		
t_2			■	■

serves to build a new component or connector by “hiding internal ports”

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hiding operator for constraint automata:

given a CA $\mathcal{A} = (Q, \mathcal{N}, \longrightarrow, Q_0)$ and port $A \in \mathcal{N}$

$\mathcal{A} \setminus A \stackrel{\text{def}}{=} (Q, \mathcal{N} \setminus \{A\}, \longrightarrow, Q_0)$ where ...

serves to build a new component or connector by “hiding internal ports”

hiding operator for constraint automata:

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$\mathcal{A} \setminus A \stackrel{\text{def}}{=} (Q, \mathcal{N} \setminus \{A\}, \longrightarrow, Q_0)$ where

$$\frac{q \xrightarrow{N, g} p \text{ in } \mathcal{A}}{q \xrightarrow{N', g'} p \text{ in } \mathcal{A} \setminus A} \quad \begin{array}{l} N' = N \setminus \{A\} \\ g' = \exists d. g[d_A/d] \end{array}$$

serves to build a new component or connector by “hiding internal ports”

hiding operator for constraint automata:

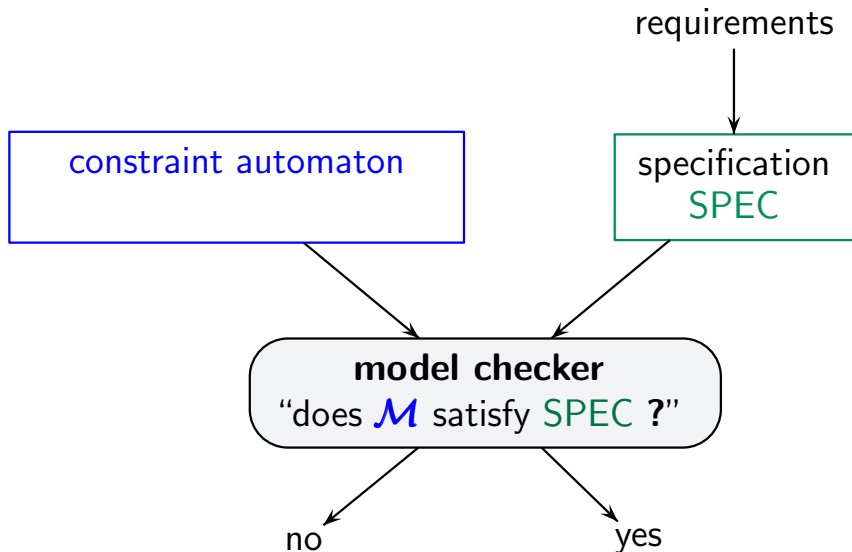
given a CA $\mathcal{A} = (Q, \mathcal{N}, \longrightarrow, Q_0)$ and port $A \in \mathcal{N}$

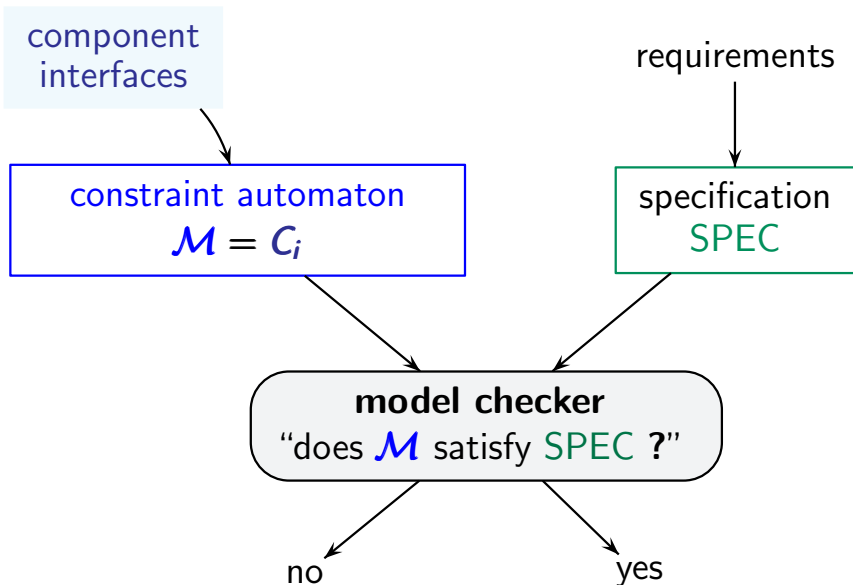
$\mathcal{A} \setminus A \stackrel{\text{def}}{=} (Q, \mathcal{N} \setminus \{A\}, \longrightarrow, Q_0)$ where

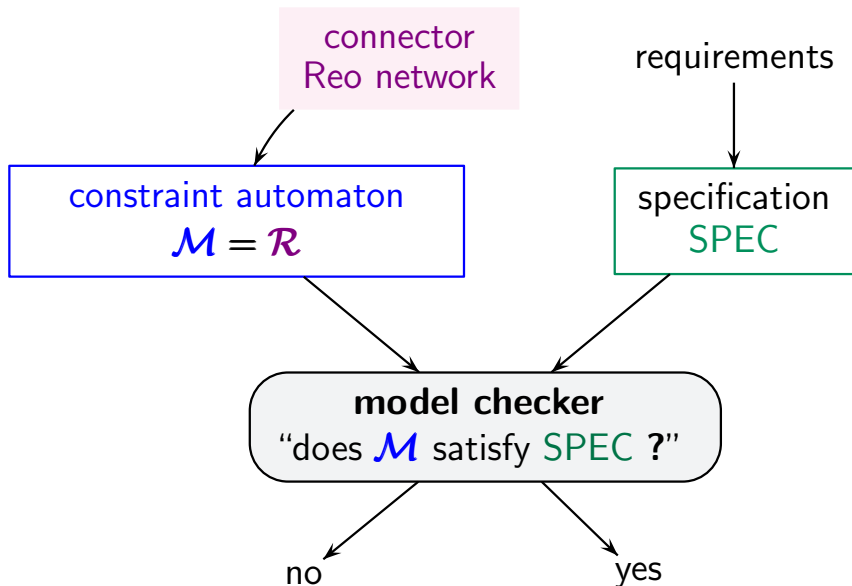
$$\frac{q \xrightarrow{N, g} p \text{ in } \mathcal{A}}{q \xrightarrow{N', g'} p \text{ in } \mathcal{A} \setminus A} \quad \begin{array}{l} N' = N \setminus \{A\} \\ g' = \exists d. g[d_A/d] \end{array}$$

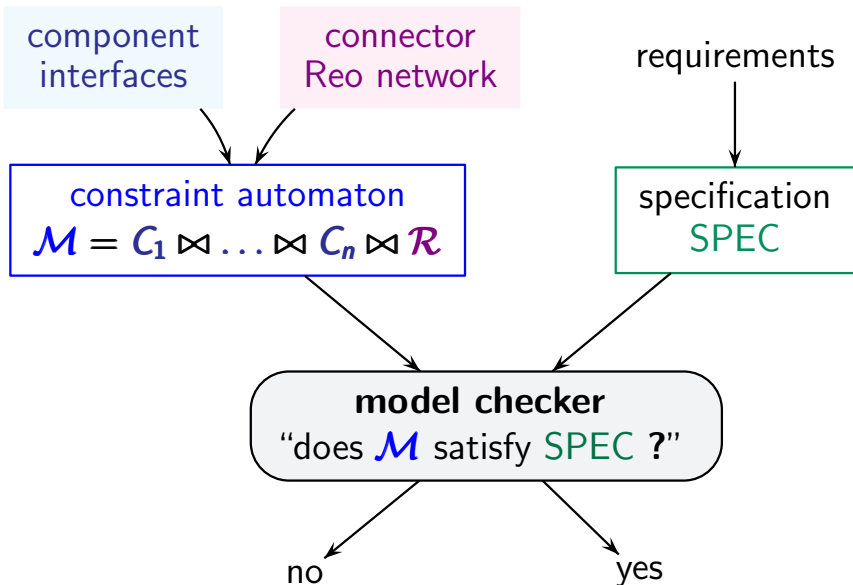
variant: additionally transitive closure over the “empty” (internal) transitions

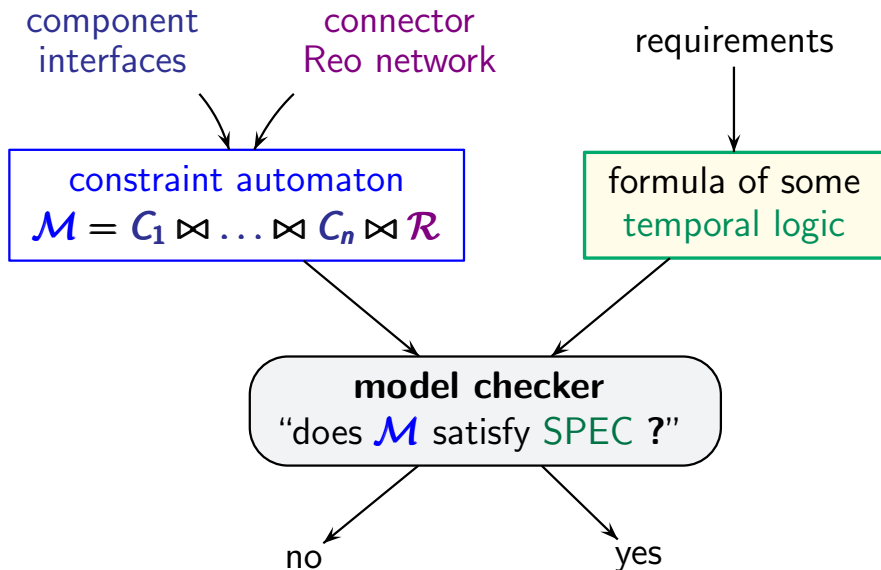
- 1 Modelling components and connectors
 - constraint automata (CA)
 - coordination language Reo
- 2 **Model checking with CA**
 - Linear Temporal Logic
 - Alternating Stream Logic
- 3 Synthesis of connectors











- 1 Modelling components and connectors
constraint automata (CA)
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- 2 **Model checking with CA**
Linear Temporal Logic ←
Alternating Stream Logic
- 3 Synthesis of connectors

linear-time logic LTL with I/O-constraints,
adapted to the CA framework

- **linear temporal logic (LTL)** [Pnueli '77]
temporal modalities over atomic propositions
to express **safety, liveness properties**
- **regular expressions** for specifying conditions on
the **interactions** of components/connectors
similar to dynamic LTL [Henriksen, Thiagarajan'99]

$$\varphi ::= \textit{true} \mid a \mid \varphi_1 \wedge \varphi_2 \mid \neg \varphi$$

$$\varphi ::= \text{true} \mid \textcolor{blue}{a} \mid \varphi_1 \wedge \varphi_2 \mid \neg \varphi$$

↑
atomic
proposition

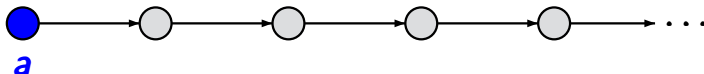
$$\varphi ::= \text{true} \mid \textcolor{blue}{a} \mid \varphi_1 \wedge \varphi_2 \mid \neg \varphi$$

↑
atomic
proposition

i.e., local condition on the states of a CA

“FIFO buffer is full”

“ $x < 3$ for integer variable x ”

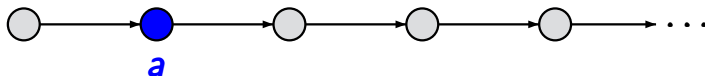


$$\varphi ::= \text{true} \mid \textcolor{blue}{a} \mid \varphi_1 \wedge \varphi_2 \mid \neg \varphi \mid \bigcirc \varphi$$

↑
atomic
proposition

↑
next

$\varphi = \bigcirc \textcolor{blue}{a}$:



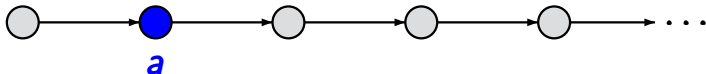
$$\varphi ::= \text{true} \mid \textcolor{blue}{a} \mid \varphi_1 \wedge \varphi_2 \mid \neg \varphi \mid \bigcirc \varphi \mid \varphi_1 \text{U} \varphi_2$$

↑
atomic
proposition

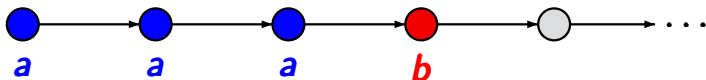
↑
next

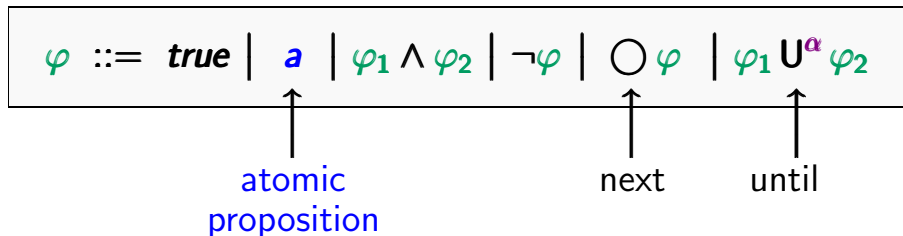
↑
until

$\varphi = \bigcirc \textcolor{blue}{a}$:

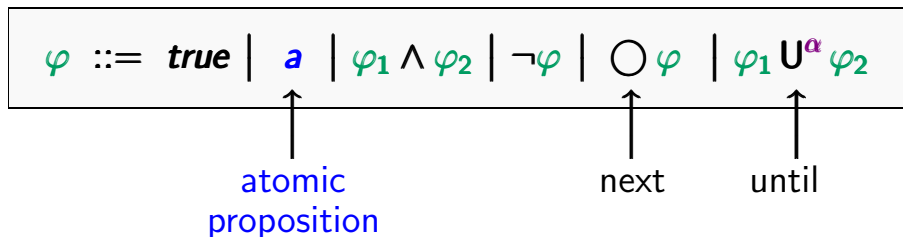


$\varphi = \textcolor{blue}{a} \text{U} \textcolor{red}{b}$:





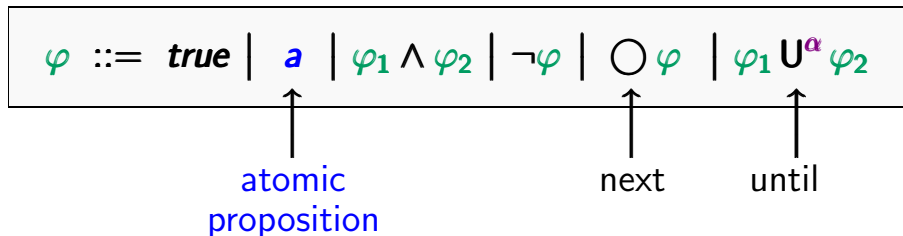
$\mathbf{U}^\alpha \hat{=}$ until indexed by a **stream expression α**



$U^\alpha \hat{=}$ until indexed by a stream expression α , i.e.,

regular expression specifying a set of finite data streams


$$\alpha ::= \text{ioc} \mid \alpha_1; \alpha_2 \mid \alpha_1 \cup \alpha_2 \mid \alpha^*$$



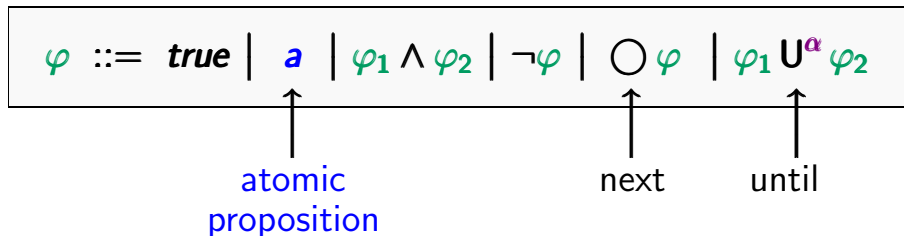
$\text{U}^{\alpha} \triangleq$ until indexed by a stream expression α , i.e.,

regular expression specifying a set of finite data streams

$\alpha ::= \textcolor{violet}{ioc} \mid \alpha_1; \alpha_2 \mid \alpha_1 \cup \alpha_2 \mid \alpha^*$



I/O-constraint, i.e., Boolean condition that specifies conditions on the active ports and their I/O-operations

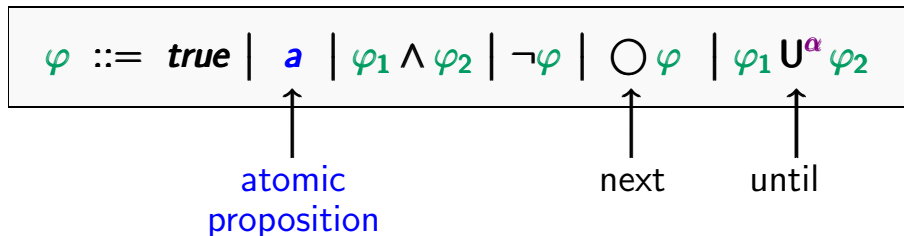


$\mathbf{U}^\alpha \triangleq$ until indexed by a stream expression α , i.e.,

regular expression specifying a set of finite data streams

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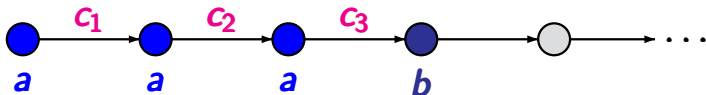
semantics of α : regular language $\mathcal{L}(\alpha)$
 (set of finite data streams)

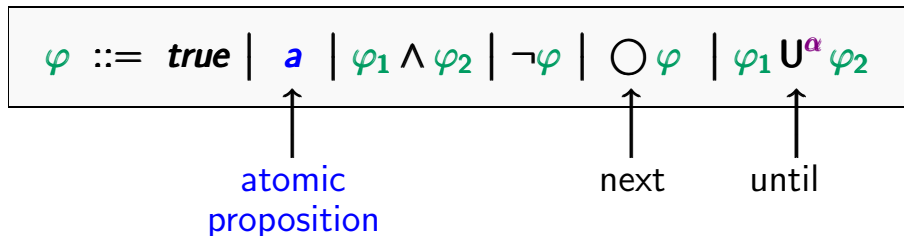


$\mathbf{U}^\alpha \hat{=}$ until indexed by a stream expression α , i.e.,

$$\varphi = a \mathbf{U}^\alpha b$$

$$c_1 c_2 c_3 \in \mathcal{L}(\alpha)$$

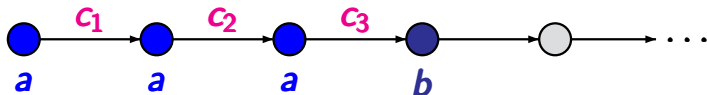




$\mathbf{U}^\alpha \hat{=}$ until indexed by a stream expression α , i.e.,

$$\varphi = a \mathbf{U}^\alpha b$$

$$c_1 c_2 c_3 \in \mathcal{L}(\alpha)$$



“standard until”: $\varphi_1 \mathbf{U} \varphi_2 \hat{=} \varphi_1 \mathbf{U}^{\text{true}^*} \varphi_2$

$$\varphi ::= \textit{true} \mid a \mid \varphi_1 \wedge \varphi_2 \mid \neg \varphi \mid \bigcirc \varphi \mid \varphi_1 \mathbf{U}^{\alpha} \varphi_2$$

derived operators:

$\forall, \rightarrow, \dots$ as usual

$$\varphi ::= \text{true} \mid a \mid \varphi_1 \wedge \varphi_2 \mid \neg \varphi \mid \bigcirc \varphi \mid \varphi_1 \mathbf{U}^{\alpha} \varphi_2$$

derived operators:

$\forall, \rightarrow, \dots$ as usual

$$\Diamond \varphi \stackrel{\text{def}}{=} \text{true} \mathbf{U} \varphi \text{ eventually}$$

$$\varphi ::= \text{true} \mid a \mid \varphi_1 \wedge \varphi_2 \mid \neg \varphi \mid \bigcirc \varphi \mid \varphi_1 \mathbf{U}^{\alpha} \varphi_2$$

derived operators:

$\forall, \rightarrow, \dots$ as usual

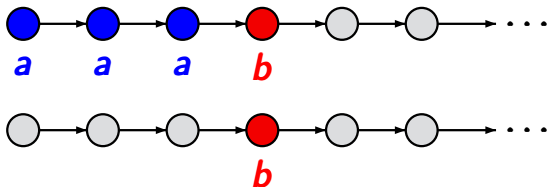
until operator

$a \mathbf{U} b$

eventually

$\Diamond b$

$$\Diamond \varphi \stackrel{\text{def}}{=} \text{true} \mathbf{U} \varphi \text{ eventually}$$



$$\varphi ::= \text{true} \mid a \mid \varphi_1 \wedge \varphi_2 \mid \neg \varphi \mid \bigcirc \varphi \mid \varphi_1 \mathbf{U}^{\alpha} \varphi_2$$

derived operators:

$\forall, \rightarrow, \dots$ as usual

until operator

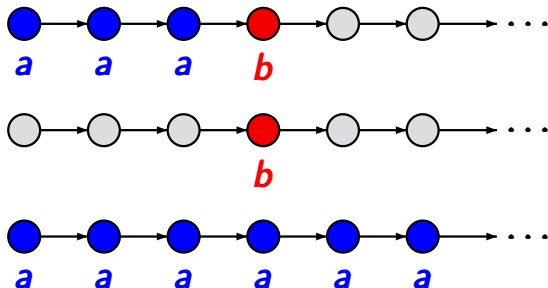
$a \mathbf{U} b$

eventually

$\Diamond b$

always

$\Box a$



$$\varphi ::= \text{true} \mid a \mid \varphi_1 \wedge \varphi_2 \mid \neg \varphi \mid \bigcirc \varphi \mid \varphi_1 \mathbf{U}^{\alpha} \varphi_2$$

derived operators:

$\forall, \rightarrow, \dots$ as usual

$$\Diamond \varphi \stackrel{\text{def}}{=} \text{true} \mathbf{U} \varphi \quad \text{eventually}$$

$$\Box \varphi \stackrel{\text{def}}{=} \neg \Diamond \neg \varphi \quad \text{always}$$

infinitely often $\Box \Diamond \varphi$

eventually forever $\Diamond \Box \varphi$

$$\varphi ::= \text{true} \mid a \mid \varphi_1 \wedge \varphi_2 \mid \neg \varphi \mid \bigcirc \varphi \mid \varphi_1 \text{U}^\alpha \varphi_2$$

$$\langle \alpha \rangle \varphi \stackrel{\text{def}}{=} \text{true} \text{U}^\alpha \varphi$$

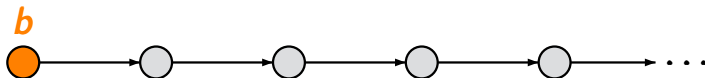
$$\varphi ::= \text{true} \mid a \mid \varphi_1 \wedge \varphi_2 \mid \neg \varphi \mid \bigcirc \varphi \mid \varphi_1 \mathbf{U}^\alpha \varphi_2$$

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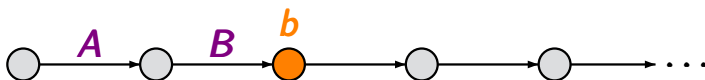
$$\varphi = \langle (A; B)^* \rangle b :$$



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$$\varphi ::= \text{true} \mid a \mid \varphi_1 \wedge \varphi_2 \mid \neg \varphi \mid \bigcirc \varphi \mid \varphi_1 U^{\alpha} \varphi_2$$

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given an execution $\pi = q_0 \xrightarrow{c_1} q_1 \xrightarrow{c_2} \dots$ in a CA:

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$$\pi \models \bigcirc \varphi \quad \text{iff} \quad \text{suffix}(\pi, 1) \models \varphi$$



$$\text{suffix}(\pi, 1) = q_1 \xrightarrow{c_2} q_2 \xrightarrow{c_3} \dots$$

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$\pi \models \varphi_1 \mathbf{U}^\alpha \varphi_2$ iff there exists a finite prefix σ of π with $\text{stream}(\sigma) \in \mathcal{L}(\alpha)$ and ...

if $|\sigma| = n$ then $\text{stream}(\sigma) = c_1 c_2 \dots c_n$

given an execution $\pi = q_0 \xrightarrow{c_1} q_1 \xrightarrow{c_2} \dots$ in a CA:

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$\text{suffix}(\pi, |\sigma|) \models \varphi_2$ and

$\text{suffix}(\pi, i) \models \varphi_1$ for $0 \leq i < |\sigma|$

given an execution $\pi = q_0 \xrightarrow{c_1} q_1 \xrightarrow{c_2} \dots$ in a CA:

$$\pi \models \Diamond \varphi \quad \text{iff} \quad \begin{array}{c} \vdots \\ \text{suffix}(\pi, i) \models \varphi \text{ for some } i \geq 0 \end{array}$$

“eventually φ ”

given an execution $\pi = q_0 \xrightarrow{c_1} q_1 \xrightarrow{c_2} \dots$ in a CA:

$$\begin{array}{ll} \vdots & \\ \pi \models \Diamond \varphi & \text{iff } \text{suffix}(\pi, i) \models \varphi \text{ for some } i \geq 0 \\ \pi \models \Box \varphi & \text{iff } \text{suffix}(\pi, i) \models \varphi \text{ for all } i \geq 0 \end{array}$$

“always φ ”

given an execution $\pi = q_0 \xrightarrow{c_1} q_1 \xrightarrow{c_2} \dots$ in a CA:

$$\begin{aligned} & \vdots \\ \pi \models \Diamond \varphi & \quad \text{iff} \quad \text{suffix}(\pi, i) \models \varphi \text{ for some } i \geq 0 \\ \pi \models \Box \varphi & \quad \text{iff} \quad \text{suffix}(\pi, i) \models \varphi \text{ for all } i \geq 0 \\ \pi \models \langle \alpha \rangle \varphi & \quad \text{iff} \quad \text{there exists a finite prefix } \sigma \text{ of } \pi \text{ s.t.} \\ & \quad \text{stream}(\sigma) \in \mathcal{L}(\alpha) \quad \text{and} \\ & \quad \text{suffix}(\pi, |\sigma|) \models \varphi \end{aligned}$$

$$\langle \alpha \rangle \varphi \stackrel{\text{def}}{=} \text{true} \mathbf{U}^\alpha \varphi$$

given an execution $\pi = q_0 \xrightarrow{c_1} q_1 \xrightarrow{c_2} \dots$ in a CA:

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given: finite constraint automaton \mathcal{A}
 LTL_{IO} formula φ

question: does $\mathcal{A} \models \varphi$ hold ?

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given: finite constraint automaton \mathcal{A}
 LTL_{IO} formula φ

question: does $\mathcal{A} \models \varphi$ hold ?



$\mathcal{A} \models \varphi$ iff for all executions π in \mathcal{A} we have: $\pi \models \varphi$
iff there is no execution π of \mathcal{A}
such that $\pi \models \neg\varphi$

constraint
automaton \mathcal{A}

LTL_{IO} formula φ

constraint
automaton \mathcal{A}

LTL_{IO} formula φ



nondeterministic Büchi
automaton \mathcal{B} for $\neg\varphi$

constraint
automaton \mathcal{A}

LTL_{IO} formula φ



nondeterministic Büchi
automaton \mathcal{B} for $\neg\varphi$

NBA like non-deterministic finite automaton (NFA)
with set of accepting states F

run $q_0 q_1 q_2 \dots$ for an infinite input string $c_1 c_2 c_3 \dots$
is accepting iff $q_i \in F$ for infinitely many $i \geq 0$

constraint
automaton \mathcal{A}

LTL_{IO} formula φ

nondeterministic Büchi
automaton \mathcal{B} for $\neg\varphi$

analysis of the product-CA $\mathcal{A} \times \mathcal{B}$

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$\neg\exists\pi$
yes, $\mathcal{A} \models \varphi$

constraint
automaton \mathcal{A}

LTL_{IO} formula φ

nondeterministic Büchi
automaton \mathcal{B} for $\neg\varphi$

analysis of the product-CA $\mathcal{A} \times \mathcal{B}$
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$\neg\exists\pi$

yes, $\mathcal{A} \models \varphi$

$\exists\pi$

no, $\mathcal{A} \not\models \varphi$

π is counterexample

constraint
automaton \mathcal{A}

LTL_{IO} formula φ

$\exp(|\varphi|)$

nondeterministic Büchi
automaton \mathcal{B} for $\neg\varphi$

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$\exp(|\varphi|)$

nondeterministic Büchi
automaton \mathcal{B} for $\neg\varphi$

analysis of the product-CA $\mathcal{A} \times \mathcal{B}$
“search for accepting execution π ”

$\mathcal{O}(|\mathcal{A}| \cdot |\mathcal{B}|)$
nested DFS

$\neg\exists\pi$

yes, $\mathcal{A} \models \varphi$

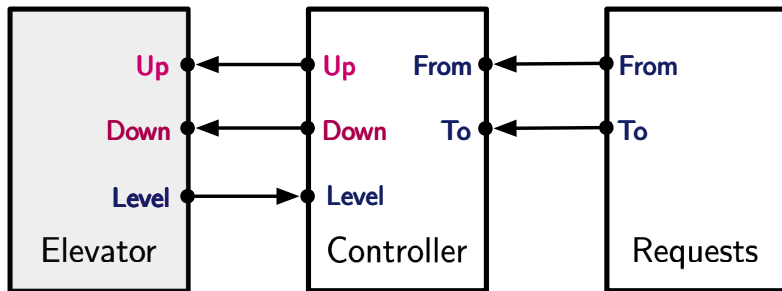
$\exists\pi$

no, $\mathcal{A} \not\models \varphi$

π is counterexample

Example: elevator system

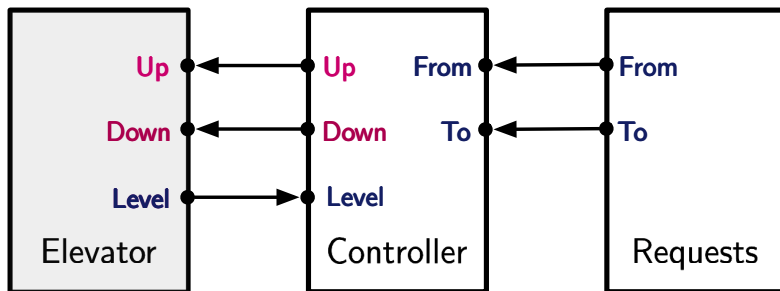
590



“elevator does not move unless **Up** or **Down**”

Example: elevator system

590

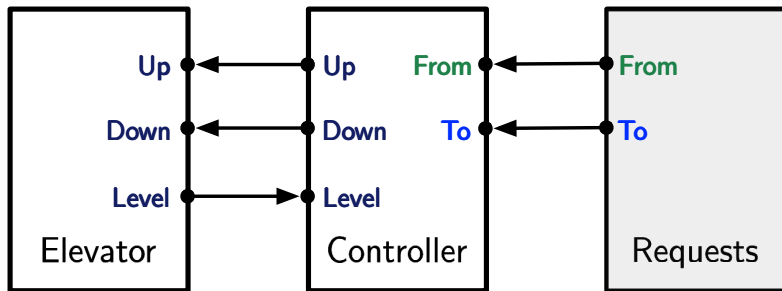


“elevator does not move unless **Up** or **Down**”

$$\bigwedge_{1 \leq i \leq k} \left(\Box \left(\text{“elevator at } i\text{”} \longrightarrow \left[(\neg \mathbf{Up} \wedge \neg \mathbf{Down})^* \right] \text{“elevator at } i\text{”} \right) \right)$$

Example: elevator system

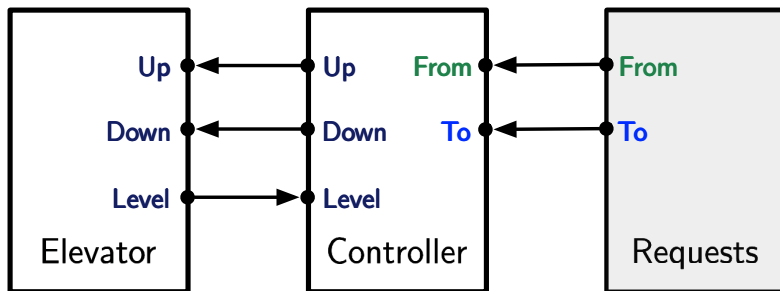
595



“each request is eventually served”

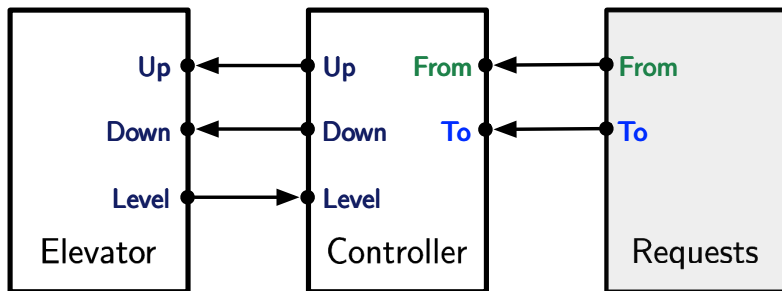
Example: elevator system

595



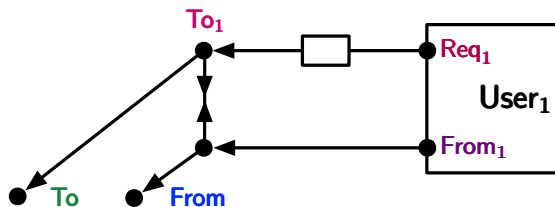
“each request is eventually served”

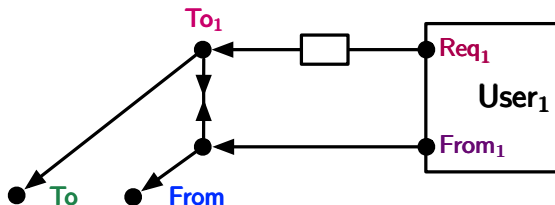
$$\bigwedge_{\substack{1 \leq i \leq k \\ 1 \leq j \leq k}} \left(\Box \left(\langle \text{From} \wedge \text{To} \wedge d_{\text{From}} = i \wedge d_{\text{To}} = j \rangle \text{true} \longrightarrow \right. \right. \\ \left. \left. \Diamond \left(\text{“elevator at } i \text{”} \wedge \Diamond \text{ “elevator at } j \text{”} \right) \right) \right)$$



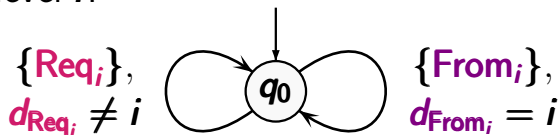
consider a refined version of the request component:

- one component for the users at each level
- port signature of user at level i :
output port Req_i , input port From_i





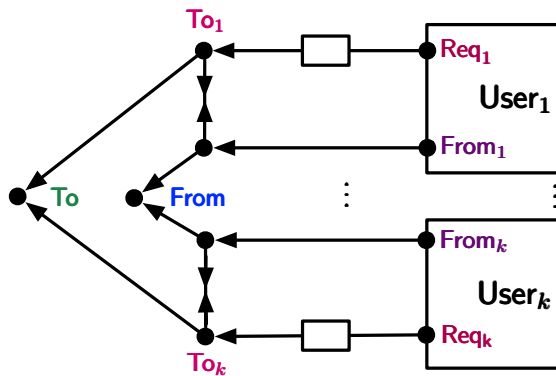
CA for **User_i** at level i :

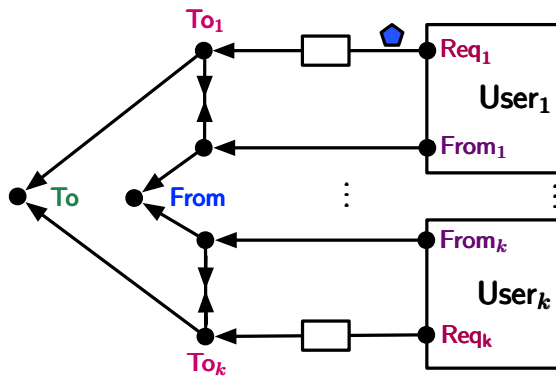


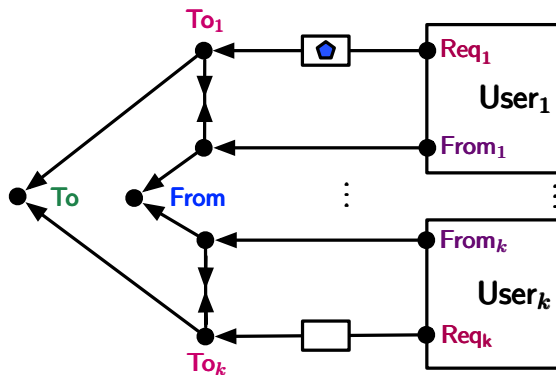
nondeterministic choice of target level

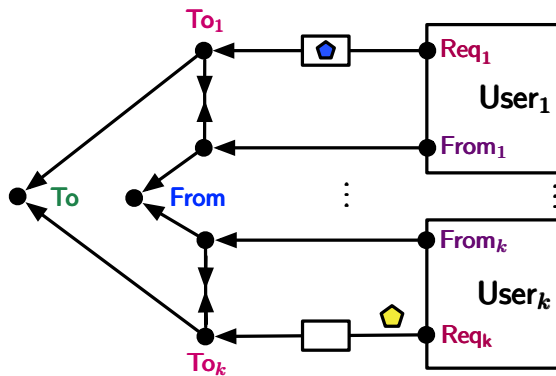
Refined request component

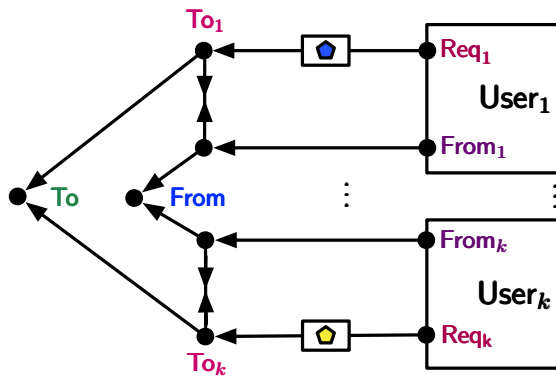
610

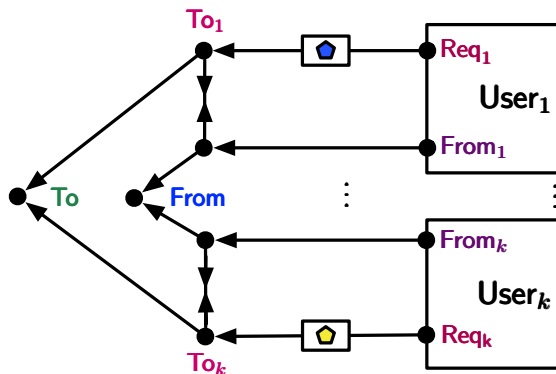




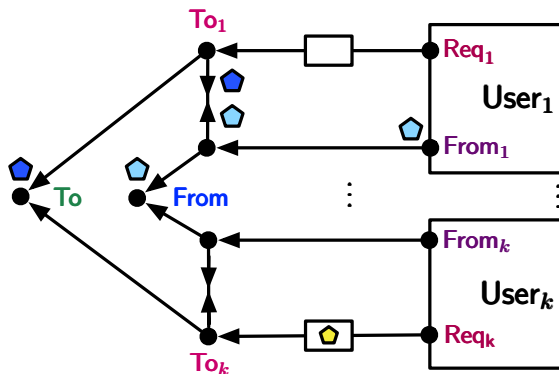




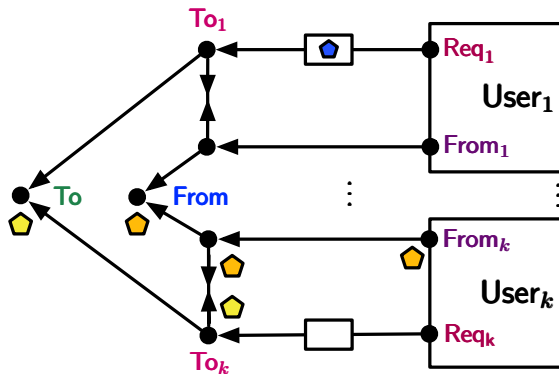




nondeterministic merge at node To between the user-requests submitted via nodes To_1, To_2, \dots, To_k



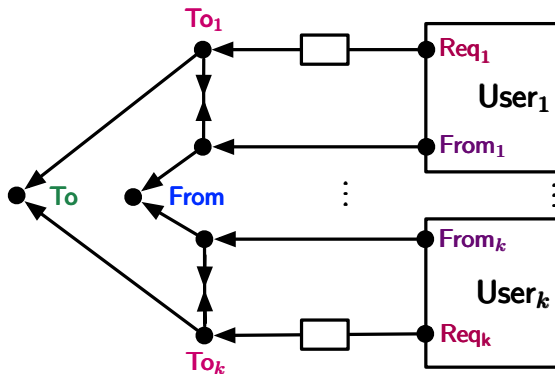
nondeterministic merge at node **To** between the user-requests submitted via nodes **To_1, To_2, \dots, To_k**



nondeterministic merge at node **To** between the user-requests submitted via nodes **To_1, To_2, \dots, To_k**

Each user will be served ?

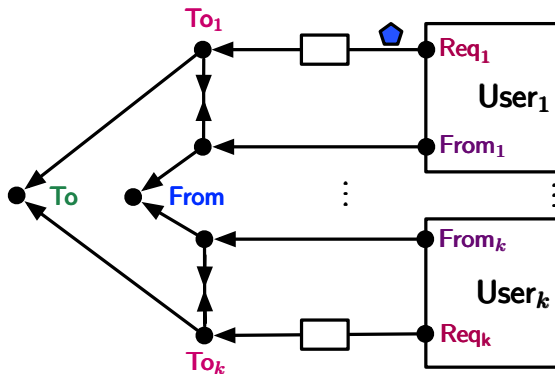
620



$$\bigwedge_{\substack{1 \leq i \leq k \\ 1 \leq j \leq k}} \left(\Box (\langle Req_i \wedge d_{Req_i} = j \rangle true \longrightarrow \Diamond (\text{"elevator at } i \text{"} \wedge \Diamond \text{"elevator at } j \text{"}))) \right) ?$$

Each user will be served ?

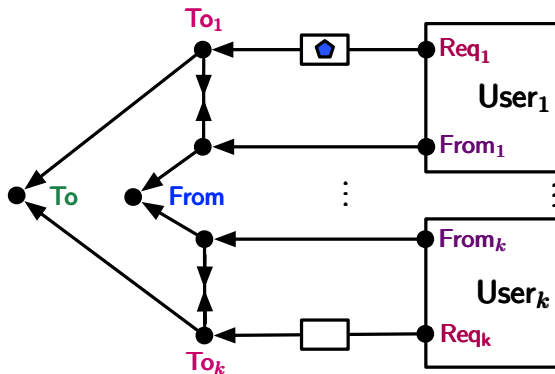
620



$$\bigwedge_{\substack{1 \leq i \leq k \\ 1 \leq j \leq k}} \left(\square (\langle Req_i \wedge d_{Req_i} = j \rangle true \longrightarrow \diamond (\text{"elevator at } i \text{"} \wedge \diamond \text{"elevator at } j \text{"}))) \right) ?$$

Each user will be served ?

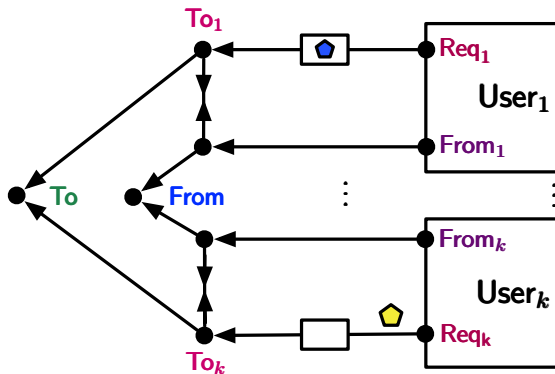
620



$$\bigwedge_{\substack{1 \leq i \leq k \\ 1 \leq j \leq k}} \left(\square (\langle Req_i \wedge d_{Req_i} = j \rangle true \longrightarrow \diamond (\text{"elevator at } i \text{"} \wedge \diamond \text{"elevator at } j \text{"}))) \right) ?$$

Each user will be served ?

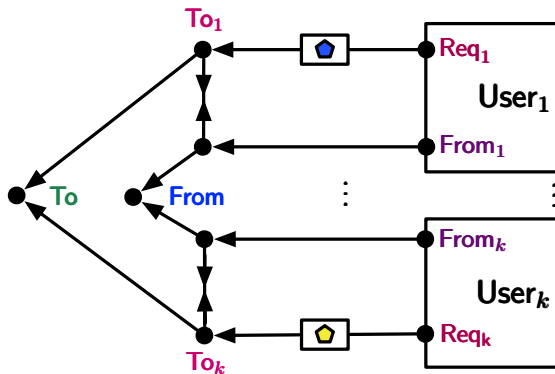
620



$$\bigwedge_{\substack{1 \leq i \leq k \\ 1 \leq j \leq k}} \left(\square (\langle Req_i \wedge d_{Req_i} = j \rangle true \longrightarrow \diamond (\text{"elevator at } i \text{"} \wedge \diamond \text{"elevator at } j \text{"}))) \right) ?$$

Each user will be served ?

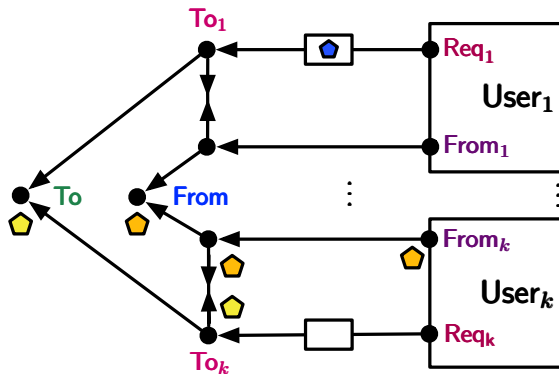
620



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Each user will be served ?

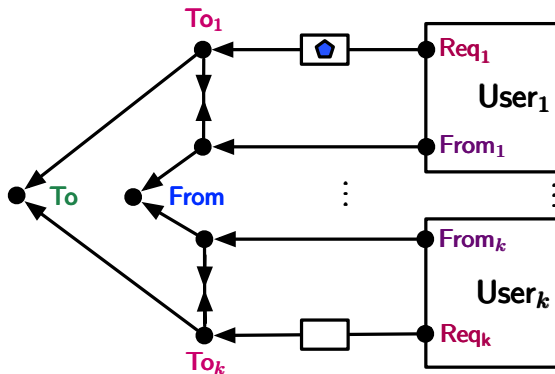
620



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Each user will be served ?

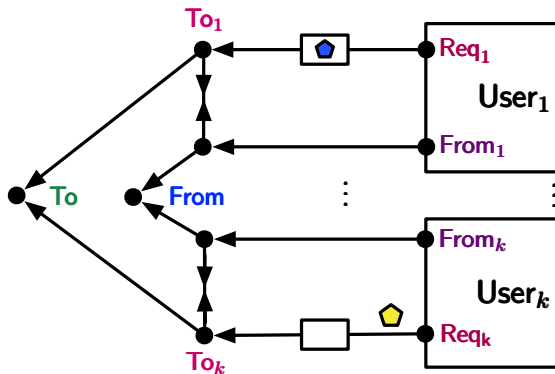
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Each user will be served ?

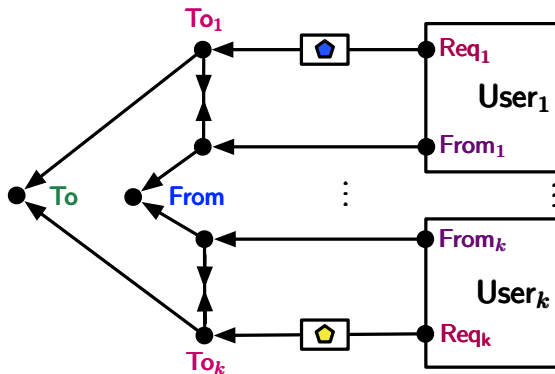
620



$$\bigwedge_{\substack{1 \leq i \leq k \\ 1 \leq j \leq k}} \left(\square (\langle Req_i \wedge d_{Req_i} = j \rangle true \longrightarrow \diamond (\text{"elevator at } i \text{"} \wedge \diamond \text{"elevator at } j \text{"}))) \right) ?$$

Each user will be served ?

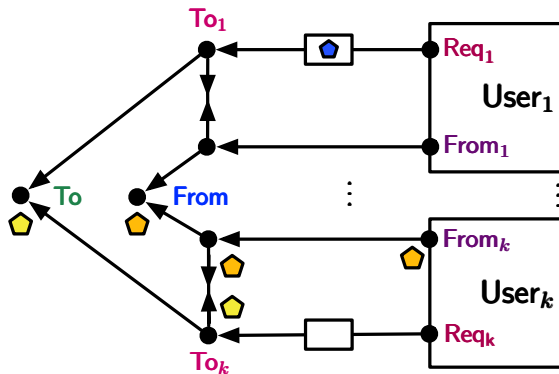
620



$$\bigwedge_{\substack{1 \leq i \leq k \\ 1 \leq j \leq k}} \left(\Box (\langle Req_i \wedge d_{Req_i} = j \rangle true \longrightarrow \Diamond (\text{"elevator at } i \text{"} \wedge \Diamond \text{"elevator at } j \text{"}))) \right) ?$$

Each user will be served ?

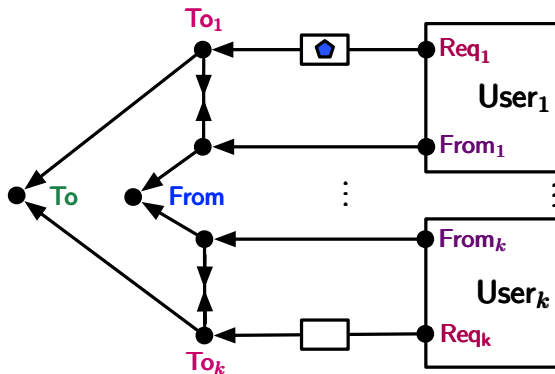
620



$$\bigwedge_{\substack{1 \leq i \leq k \\ 1 \leq j \leq k}} \left(\Box (\langle Req_i \wedge d_{Req_i} = j \rangle true \longrightarrow \Diamond (\text{"elevator at } i \text{"} \wedge \Diamond \text{"elevator at } j \text{"}))) \right) ?$$

Each user will be served ? ... no

620



unfair merge at node **To** is possible

Liveness properties often cannot be established for nondeterministic system models, although they are expected to hold.

Nondeterministic system models can contain unrealistic behavior, e.g.,

- a certain process is never scheduled

- a request is ignored forever

Liveness properties often cannot be established for nondeterministic system models, although they are expected to hold.

Nondeterministic system models can contain **unrealistic behavior**, e.g.,

- a certain process is **never scheduled**

- a request is **ignored forever**

specify appropriate **fairness assumptions**,
consider only **fair executions** for the analysis,
and ignore the unfair ones

unconditional fairness:

$$\Box \Diamond \text{engaged}(P)$$

weak fairness:

$$\Diamond \Box \text{enabled}(P) \longrightarrow \Box \Diamond \text{engaged}(P)$$

strong fairness:

$$\Box \Diamond \text{enabled}(P) \longrightarrow \Box \Diamond \text{engaged}(P)$$

$\text{engaged}(P) \hat{=}$ process P is scheduled

$\text{enabled}(P) \hat{=}$ process P can be scheduled

unconditional fairness:

$$\Box \Diamond \text{engaged}(A)$$

weak fairness:

$$\Diamond \Box \text{enabled}(A) \longrightarrow \Box \Diamond \text{engaged}(A)$$

strong fairness:

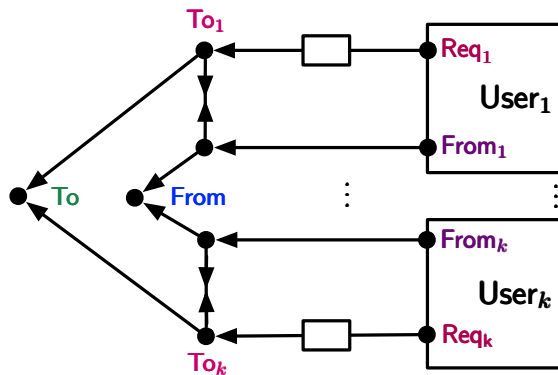
$$\Box \Diamond \text{enabled}(A) \longrightarrow \Box \Diamond \text{engaged}(A)$$

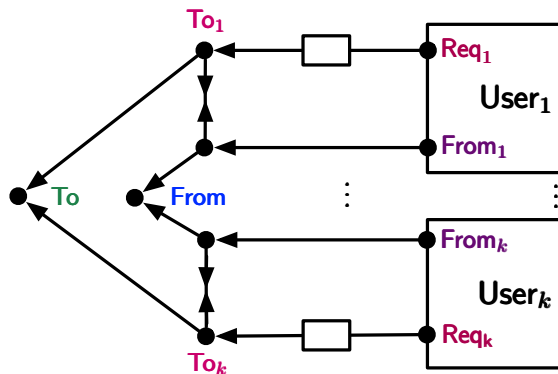
$$\text{engaged}(A) \hat{=} \langle A \rangle \text{true}$$

$\text{enabled}(A)$ iff there exists a transition of the current state where A is involved

Again: elevator request component

650

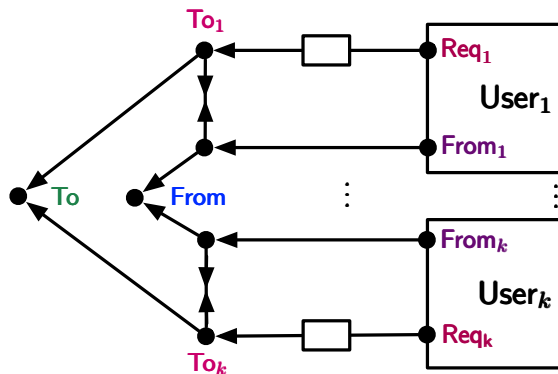




suppose that node To resolves its choices fairly:

$$\psi = \bigwedge_{1 \leq i \leq k} \left(\Box \Diamond \text{enabled}(To_i) \longrightarrow \Box \Diamond \langle To_i \rangle \text{true} \right)$$

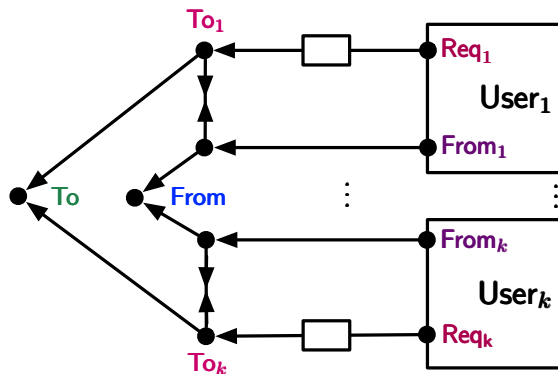
strong fairness for the nodes To_1, \dots, To_k



suppose that node To resolves its choices fairly:

$$\psi = \bigwedge_{1 \leq i \leq k} \left(\Box \Diamond \text{enabled}(To_i) \longrightarrow \Box \Diamond \langle To_i \rangle \text{true} \right)$$

“there exists a transition where To_i is active”



$$\bigwedge_{\substack{1 \leq i \leq k \\ 1 \leq j \leq k}} \left(\Box (\langle \text{Req}_i \wedge d_{\text{Req}_i} = j \rangle \text{true} \longrightarrow \Diamond (\text{"elevator at } i\text{"} \wedge \Diamond \text{"elevator at } j\text{"}))) \right)$$

holds under fairness assumption ψ

given: constraint automaton \mathcal{A}

LTL_{IO} formula φ

fairness assumptions $\psi = \bigwedge_i \psi_i$

question: does $\mathcal{A} \models \varphi$ hold under fairness assumption ψ ?

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i.e., for all executions π of \mathcal{A} :

$$\text{if } \pi \models \psi \text{ then } \pi \models \varphi \quad \longleftarrow \quad \boxed{\pi \models (\psi \rightarrow \varphi)}$$

method: use standard LTL_{IO} model checker

for the formula $\psi \rightarrow \varphi$

(or adapt the model checking procedure)

- 1 Modelling components and connectors
constraint automata (CA)
coordination language Reo
- 2 **Model checking with CA**
Linear Temporal Logic
Alternating Stream Logic ←
- 3 Synthesis of connectors

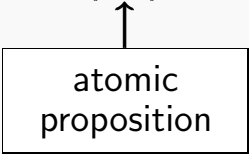
branching-time logic that combines features of

- computation tree logic (CTL) [Clarke, Emerson '81]
 - * temporal operators (safety, liveness)
- modal logic (dynamic logic PDL)
 - * regular expressions for specifying data streams and their effect

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 - * regular expressions for specifying data streams and their effect
- alternating-time temporal logic [Alur,Henz.,Kupfer.'97]
 - * CA as multi-player games
 - * reasoning about strategies of components and cooperation facilities of coalitions of components

ASL state formulas: as in CTL + ...

$$\Phi ::= \text{true} \mid a \mid \Phi_1 \wedge \Phi_2 \mid \neg \Phi \mid \exists \varphi \mid \dots$$


↑
atomic
proposition

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↑
atomic
proposition

↑
existential
path quantifier

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ASL path formulas: as in CTL + ...

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ASL state formulas: as in CTL + ATL-like quantifiers

$$\Phi ::= \text{true} \mid a \mid \Phi_1 \wedge \Phi_2 \mid \neg \Phi \mid \exists \varphi \mid \mathbb{E}_{\mathfrak{C}} \varphi$$

ASL path formulas: as in CTL + ...

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$\exists \varphi$ “there exists an execution where φ holds”

$\mathbb{E}_{\mathfrak{C}} \varphi$ “coalition \mathfrak{C} can enforce that φ holds”
no matter how the opponents behave

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where \mathfrak{c} is a **coalition**, i.e., set of I/O-ports

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derived: e.g., $\mathbb{A}_{\mathfrak{C}} \Diamond \Phi = \neg \mathbb{E}_{\mathfrak{C}} \Box \neg \Phi$

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derived: e.g., $\mathbb{A}_{\mathfrak{C}} \Diamond \Phi = \neg \mathbb{E}_{\mathfrak{C}} \Box \neg \Phi$, $\exists \varphi = \mathbb{A}_{\emptyset} \varphi$

ASL state formulas: as in CTL + ATL-like quantifiers

$$\Phi ::= \text{true} \mid a \mid \Phi_1 \wedge \Phi_2 \mid \neg \Phi \mid \exists \varphi \mid \mathbb{E}_{\alpha} \varphi \mid \mathbb{A}_{\alpha} \varphi$$

ASL path formulas: as in CTL + PDL-like expressions

$$\varphi ::= \bigcirc \Phi \mid \Phi_1 \mathbf{U} \Phi_2 \mid \langle \alpha \rangle \Phi \mid [\alpha] \Phi$$

where α is again a **regular expression** that specifies a set of finite data streams (as in **LTL_{IO}**)

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$\langle \alpha \rangle \Phi$ “there is a α -prefix that ends in a Φ -state”

$[\alpha] \Phi$ “all α -prefixes end in a Φ -state”

ASL path formulas:

$$\varphi ::= \bigcirc \Phi \mid \Phi_1 \cup \Phi_2 \mid \langle \alpha \rangle \Phi \mid [\alpha] \Phi$$

given an execution $\pi = q_0 \xrightarrow{c_1} q_1 \xrightarrow{c_2} \dots$ of a CA:

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$$\pi \models [\alpha] \Phi \quad \text{iff} \quad \text{for all finite prefixes } \sigma \text{ of } \pi: \text{stream}(\sigma) \in \mathcal{L}(\alpha) \text{ implies } \text{last}(\sigma) \models \Phi$$

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ASL state formulas:

$$\Phi ::= \underbrace{true \mid a \mid \Phi_1 \wedge \Phi_2 \mid \neg \Phi \mid \exists \varphi}_{\text{as in CTL}} \mid \mathbb{E}_{\mathbf{c}} \varphi \mid \mathbb{A}_{\mathbf{c}} \varphi$$

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for state q of a CA:

$$q \models \text{true}$$

$$q \models a \quad \text{iff} \quad "a \text{ holds in state } q"$$

$$q \models \Phi_1 \wedge \Phi_2 \quad \text{iff} \quad q \models \Phi_1 \text{ and } q \models \Phi_2$$

$$q \models \neg \Phi \quad \text{iff} \quad q \not\models \Phi$$

$$q \models \exists \varphi \quad \text{iff} \quad \text{there is an execution } \pi \text{ starting in } q \text{ such that } \pi \models \varphi$$

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strategy \mathcal{S} assigns to each finite execution σ a set of concurrent I/O-operations that contains all concurrent I/O-operations where no port in \mathfrak{c} is involved

ASL state formulas:

$$\Phi ::= \underbrace{\text{true} \mid a \mid \Phi_1 \wedge \Phi_2 \mid \neg \Phi \mid \exists \varphi}_{\text{as in CTL}} \mid \mathbb{E}_{\mathfrak{e}} \varphi \mid \mathbb{A}_{\mathfrak{e}} \varphi$$

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$q \models \mathbb{A}_{\mathfrak{e}} \varphi$ iff for all strategies \mathcal{S} for the ports $A \in \mathfrak{e}$ there exists an \mathcal{S} -execution π starting in q such that $\pi \models \varphi$

given: finite constraint automaton \mathcal{A}

ASL state formula ϕ

question: does $\mathcal{A} \models \phi$ hold ?

given: finite constraint automaton \mathcal{A}
 ASL state formula Φ

question: does $\mathcal{A} \models \Phi$ hold ?

algorithm: compute recursively the satisfaction sets

$$\text{Sat}(\Psi) = \{ q \text{ state in } \mathcal{A} : q \models \Psi \}$$

for all state subformulas Ψ of Φ

given: finite constraint automaton \mathcal{A}
 ASL state formula Φ

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algorithm: compute recursively the satisfaction sets

$$\text{Sat}(\Psi) = \{ q \text{ state in } \mathcal{A} : q \models \Psi \}$$

for all state subformulas Ψ of Φ

- treatment of $\mathbb{E}_c \Diamond \Psi$, or $\mathbb{E}_c \Box \Psi$:
iterative fixed point computation
- treatment of $\mathbb{E}_c \langle \alpha \rangle \Psi$ or $\mathbb{E}_c [\alpha] \Psi$:
via reduction to $\mathbb{E}_c \Diamond$ and or $\mathbb{E}_c \Box$, respectively

Computation of $Sat(\mathbb{E}_{\epsilon}\langle\alpha\rangle\psi)$

760

finite constraint
automaton \mathcal{A}

ASL state formula
 $\mathbb{E}_{\epsilon}\langle\alpha\rangle\psi$

Computation of $Sat(\mathbb{E}_{\epsilon}\langle\alpha\rangle\psi)$

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finite constraint
automaton \mathcal{A}

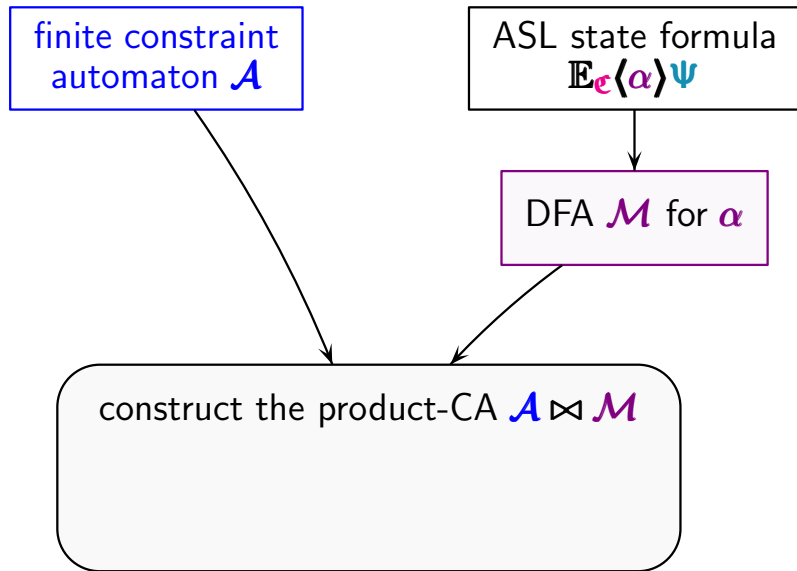
ASL state formula
 $\mathbb{E}_{\epsilon}\langle\alpha\rangle\psi$



DFA \mathcal{M} for α

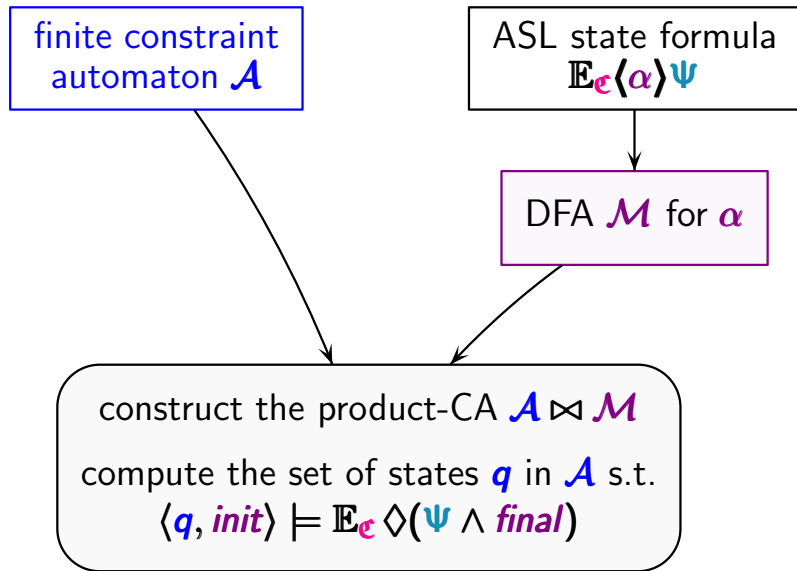
Computation of $Sat(\mathbb{E}_c\langle\alpha\rangle\psi)$

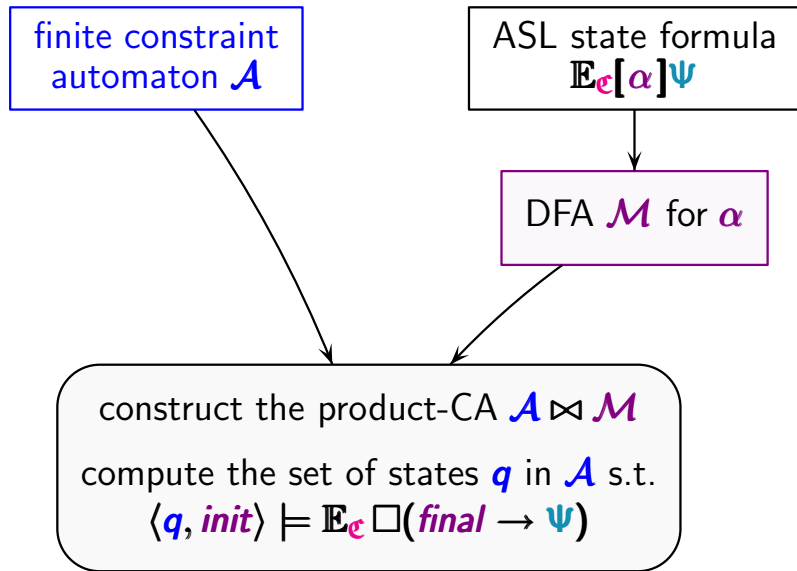
760



Computation of $Sat(\mathbb{E}_c\langle\alpha\rangle\psi)$

760





given: finite constraint automaton \mathcal{A}
 ASL state formula Φ

question: does $\mathcal{A} \models \Phi$ hold ?

complexity of the sketched algorithm:

$$\mathcal{O}(\text{size}(\mathcal{A}) \cdot \exp(k) \cdot |\Phi|)$$

where k = maximal length $|\alpha|$ of a stream expression
that appears in Φ

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exponential blow-up possible as DFA for
path subformulas $\langle \alpha \rangle \Psi$ or $[\alpha] \Psi$ are required

complexity of model checking for formulas of

- the ATL-fragment of ASL (without $\langle \alpha \rangle$, $[\alpha]$):

$$\mathcal{O}(\text{size}(\mathcal{A}) \cdot |\Phi|) \quad \longleftarrow \text{as for standard ATL}$$

complexity of model checking for formulas of

- the ATL-fragment of ASL (without $\langle \alpha \rangle$, $[\alpha]$):

$$\mathcal{O}(\text{size}(\mathcal{A}) \cdot |\Phi|) \quad \longleftarrow \text{as for standard ATL}$$

- the fragment of ASL consisting of CTL + $\exists \langle \alpha \rangle$:

$$\mathcal{O}(\text{size}(\mathcal{A}) \cdot |\Phi|) \quad \longleftarrow \text{NFA are sufficient}$$

complexity of model checking for formulas of

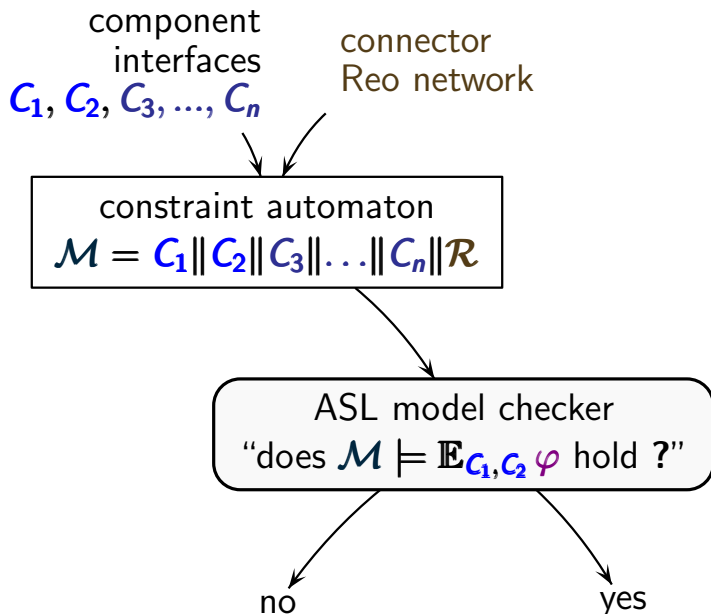
- the ATL-fragment of ASL (without $\langle \alpha \rangle$, $[\alpha]$):

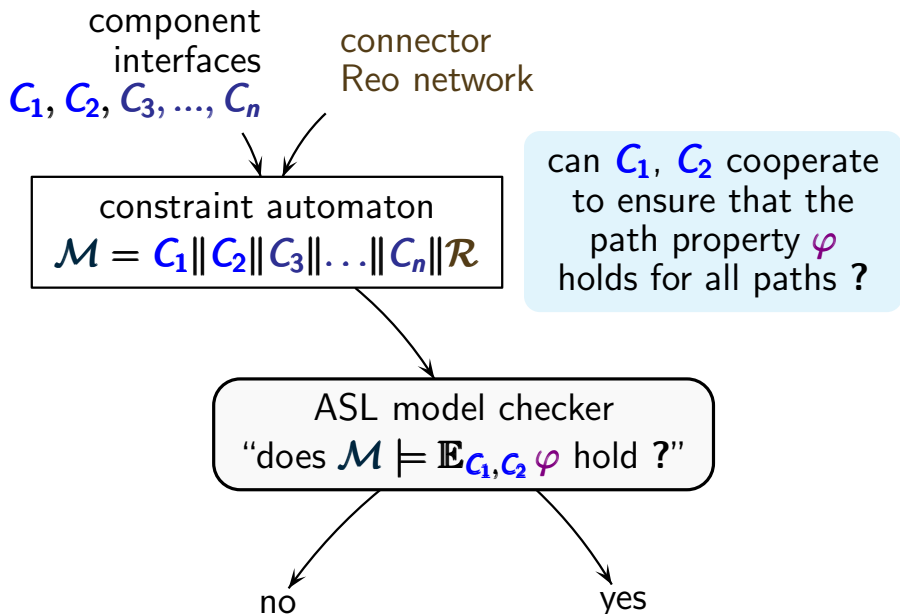
$$\mathcal{O}(\text{size}(\mathcal{A}) \cdot |\Phi|) \longleftarrow \text{as for standard ATL}$$

- the fragment of ASL consisting of CTL + $\exists \langle \alpha \rangle$:

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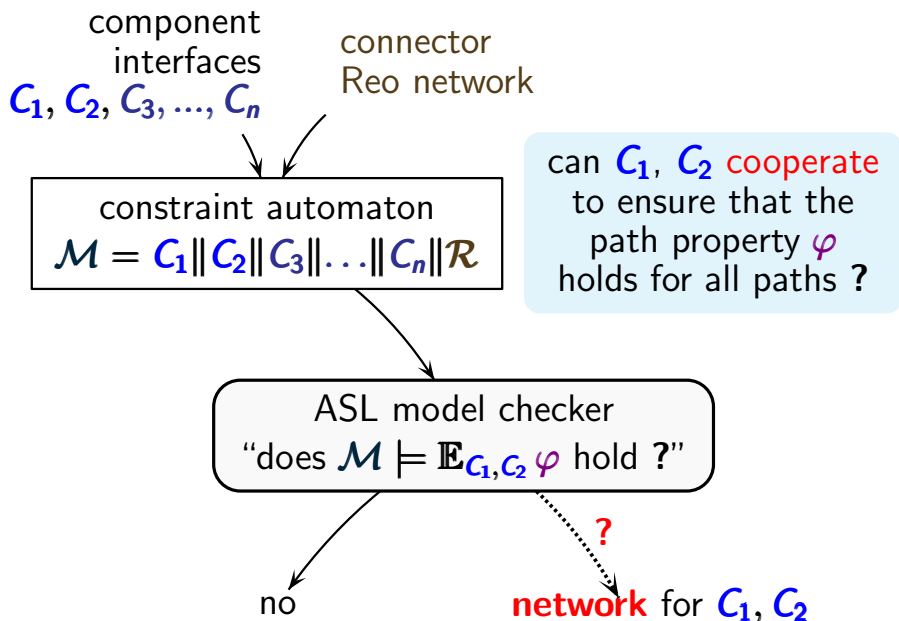
but: **PSPACE-completeness** of the model checking problem for ASL formulas of the form $\mathbb{E}_{\mathbf{c}} \langle \alpha \rangle a$ where α is given by an NFA





Synthesis of controller for C_1 and C_2 ?

780



component
interfaces
 $C_1, C_2, C_3, \dots, C_n$

can C_1, \dots, C_n cooperate
such that $C_1 \parallel \dots \parallel C_n$
is never blocked ?

constraint automaton

$$\mathcal{M} = C_1 \parallel C_2 \parallel C_3 \parallel \dots \parallel C_n$$

compatibility

[DEALFARO/HENZINGER'03]

ASL model checker

$$“\mathcal{M} \models \mathbb{E}_{C_1, \dots, C_n} \bigcirc true ?”$$

no

yes

component
interfaces
 $C_1, C_2, C_3, \dots, C_n$

do the interfaces of
 C_1, \dots, C_n meet each other
interface constraints ?

constraint automaton
 $\mathcal{M} = C_1 \parallel C_2 \parallel C_3 \parallel \dots \parallel C_n$

↑
ASL⁺ path formula
 $\varphi = \psi_1 \wedge \dots \wedge \psi_n$

ASL model checker
“ $\mathcal{M} \models \mathbb{E}_{C_1, \dots, C_n} \varphi$?”

no

yes

component
interfaces
 $C_1, C_2, C_3, \dots, C_n$

do the interfaces of
 C_1, \dots, C_n meet each other
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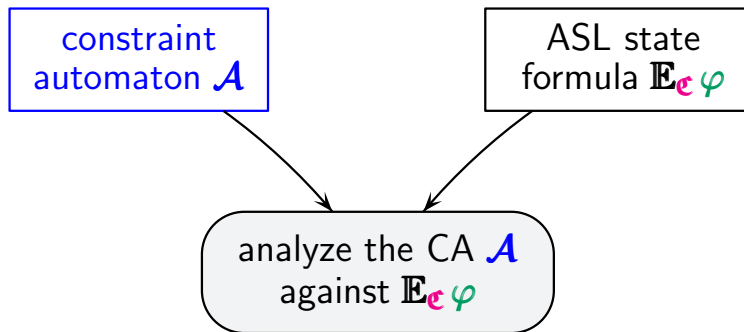
constraint automaton
 $\mathcal{M} = C_1 \parallel C_2 \parallel C_3 \parallel \dots \parallel C_n$

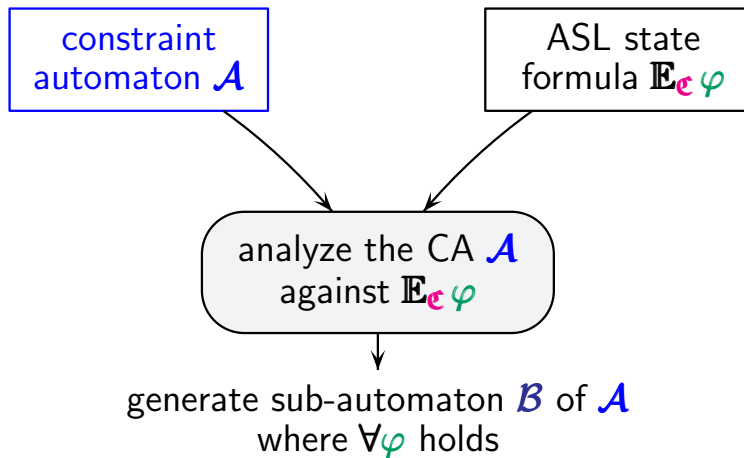
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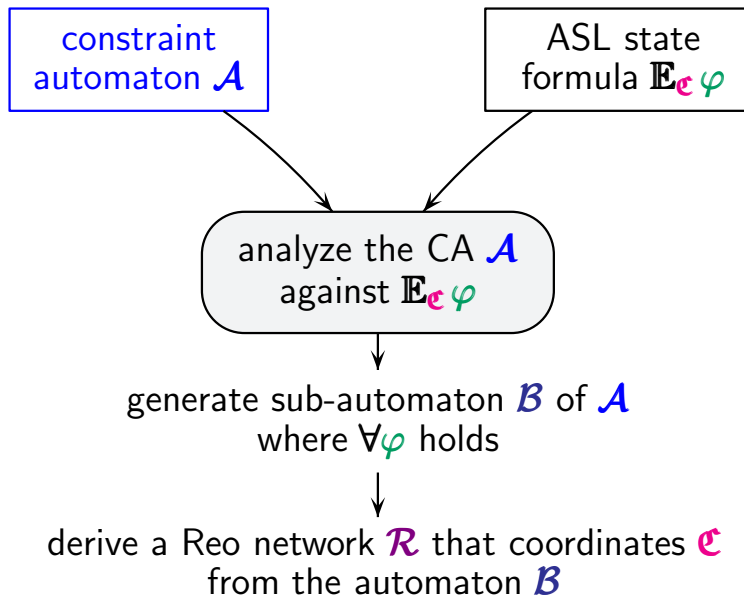
ASL model checker
“ $\mathcal{M} \models \mathbb{E}_{C_1, \dots, C_n} \varphi$?”

no

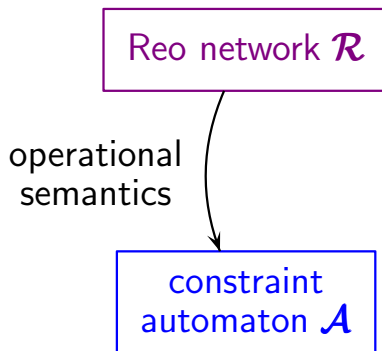
yes + **Reo network**

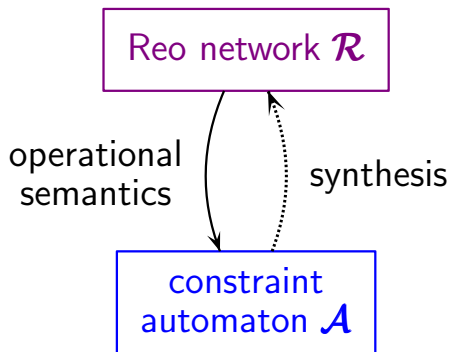


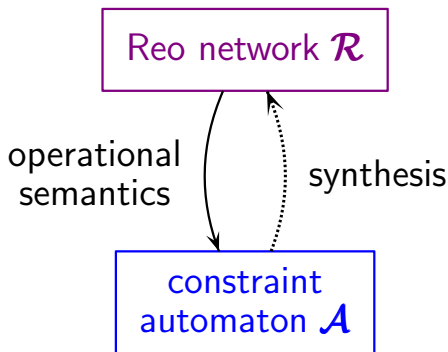




- 1 Modelling components and connectors
 - constraint automata (CA)
 - coordination language Reo
- 2 Model checking with CA
 - Linear Temporal Logic
 - Alternating Stream Logic
- 3 **Synthesis of connectors**







For each finite CA \mathcal{A} , a Reo network \mathcal{R} of size $\mathcal{O}(\text{size}(\mathcal{A}))$ can be constructed such that

$\mathcal{A} = \text{operational semantics of } \mathcal{R}$
 (up to some notion of behavioral equivalence)

given: constraint automaton $\mathcal{A} = (Q, \mathcal{N}, \longrightarrow, \{q_0\})$

where $\mathcal{N} = \mathcal{N}_{\text{in}} \cup \mathcal{N}_{\text{out}}$ (no internal ports)

task: synthesize an equivalent Reo network \mathcal{R}

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transitions \rightsquigarrow data flow in \mathcal{R}

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- current state q of \mathcal{A} is represented by a token in the FIFO buffer for q
- firing a transition in \mathcal{A} corresponds to passing the token from one FIFO to another one

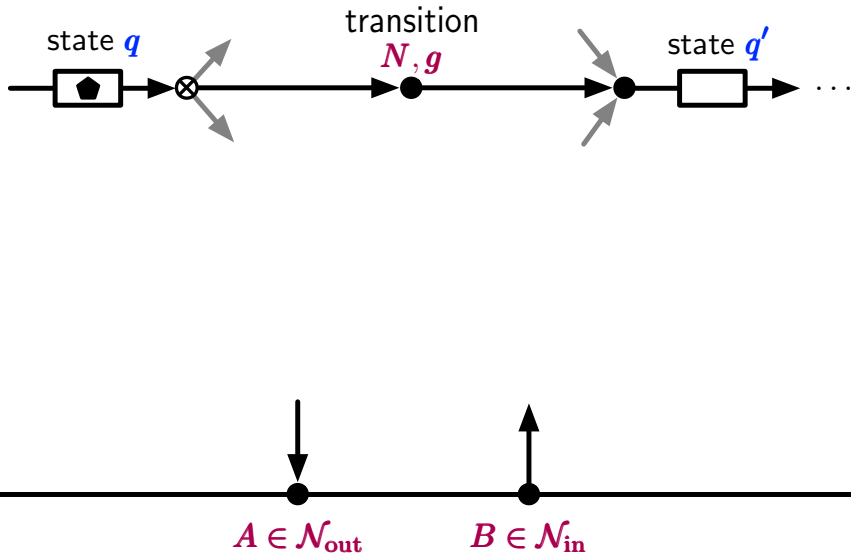
representation of transition $q \xrightarrow{N, g} q'$ in the network

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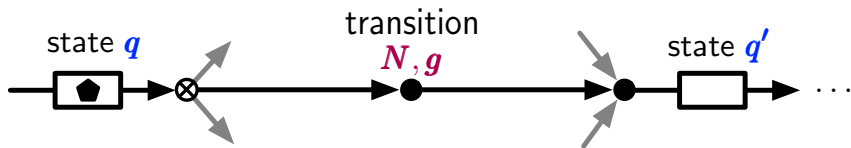
Reo network with one I/O-port
for each port in \mathcal{N}



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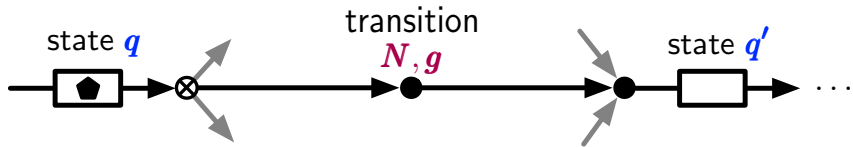


one FIFO channel for each **state** such that in each reachable configuration:

precisely one of the FIFO buffers is filled
(indicating the current state)



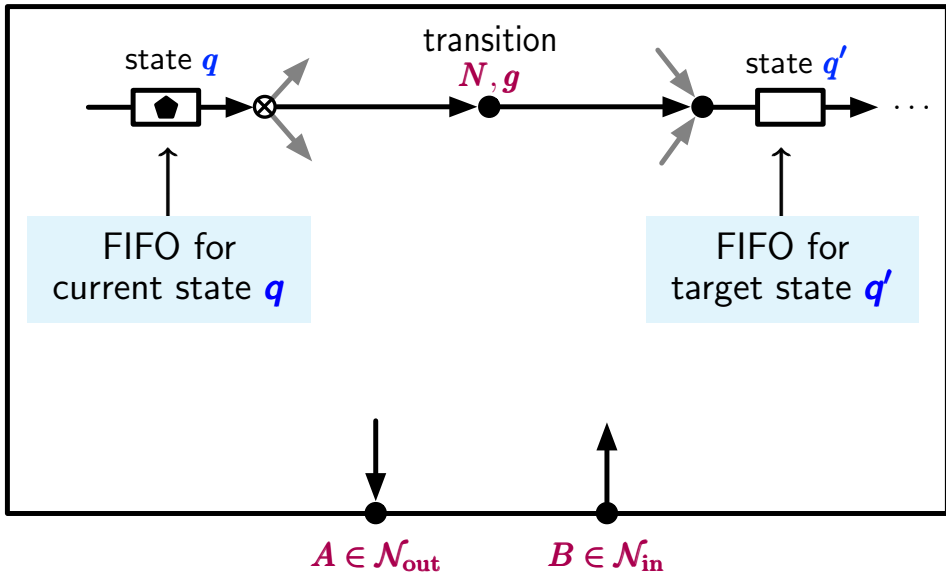
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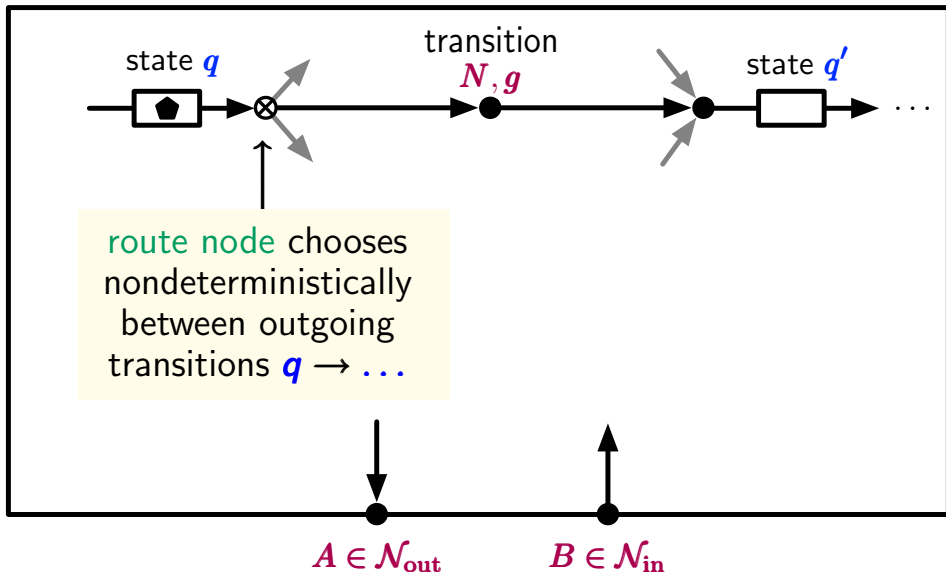
for proper treatment of self-loops $q \xrightarrow{N, g} q$:
variant of standard FIFO channels that
can send and receive token simultaneously



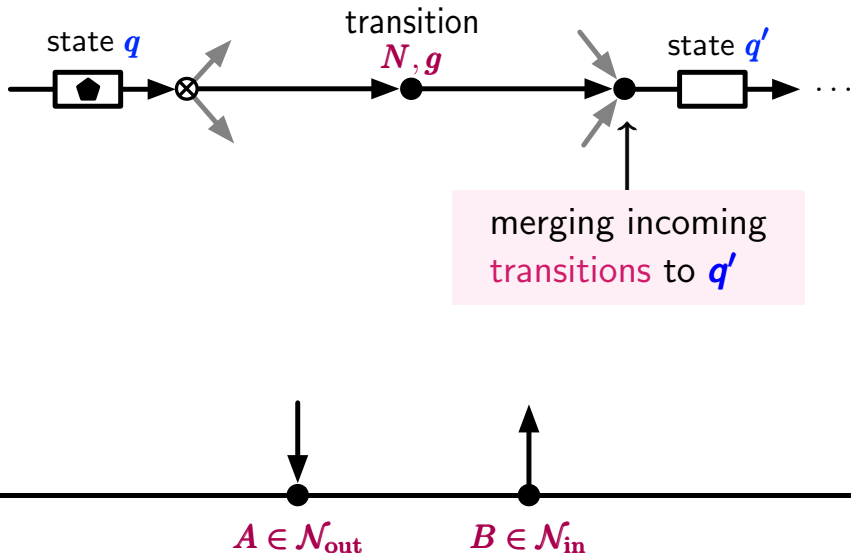
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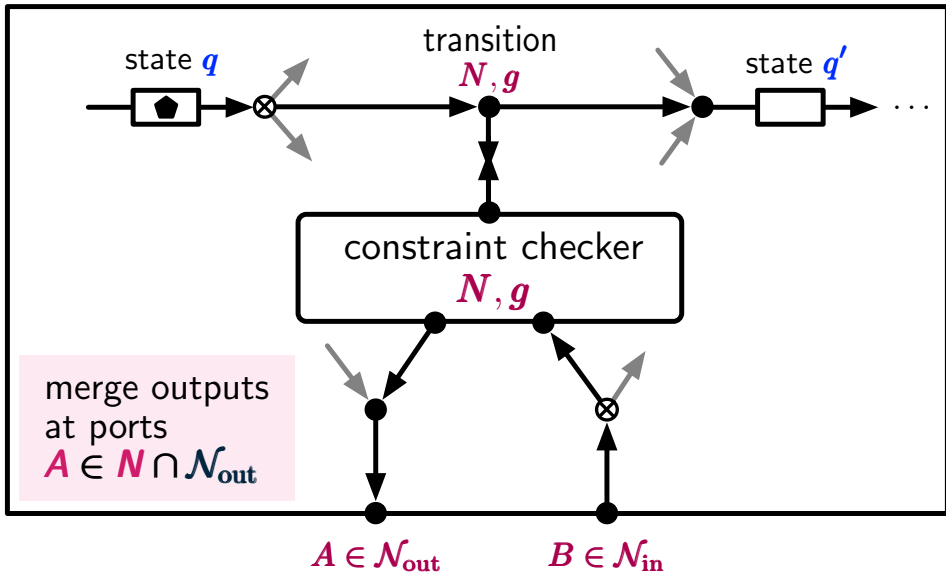
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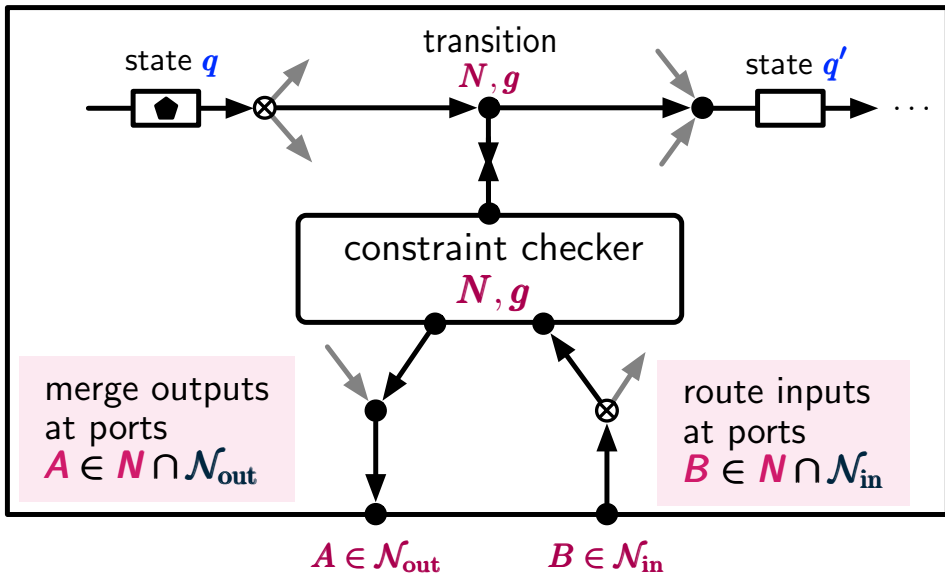
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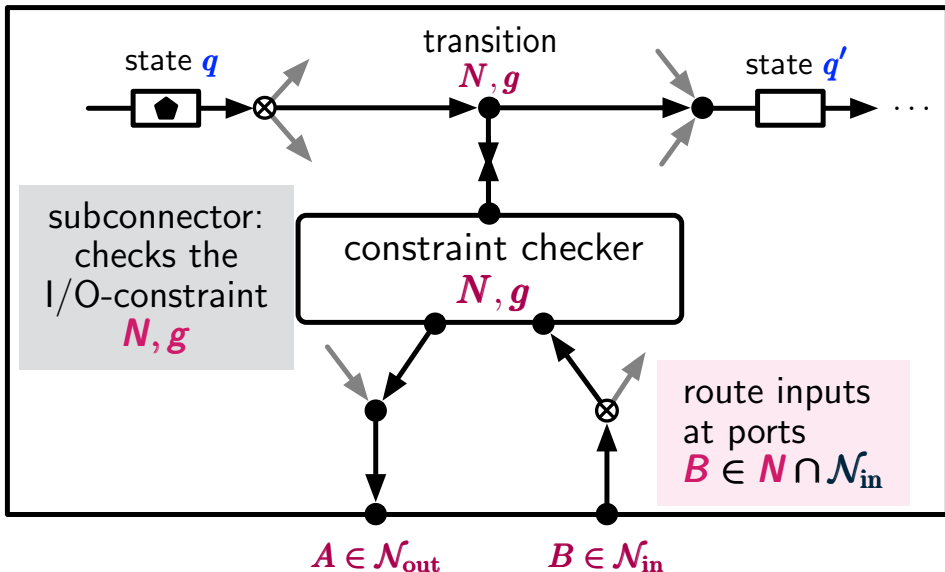
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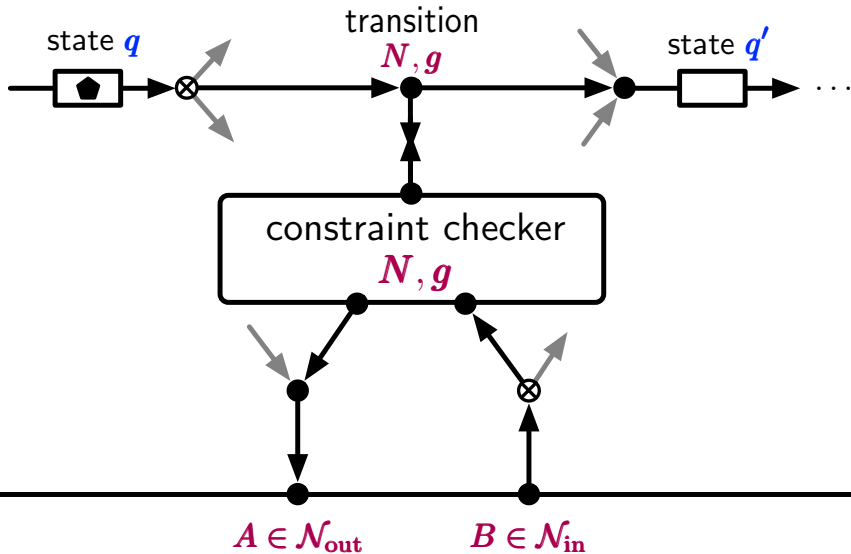
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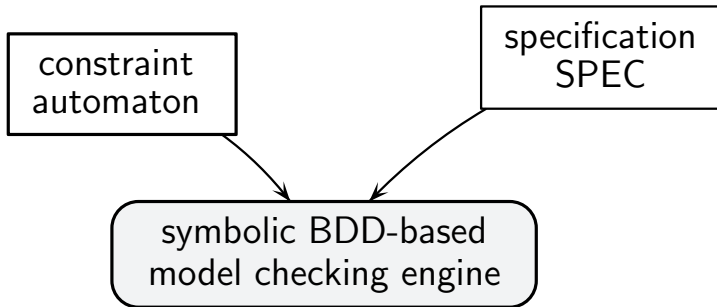
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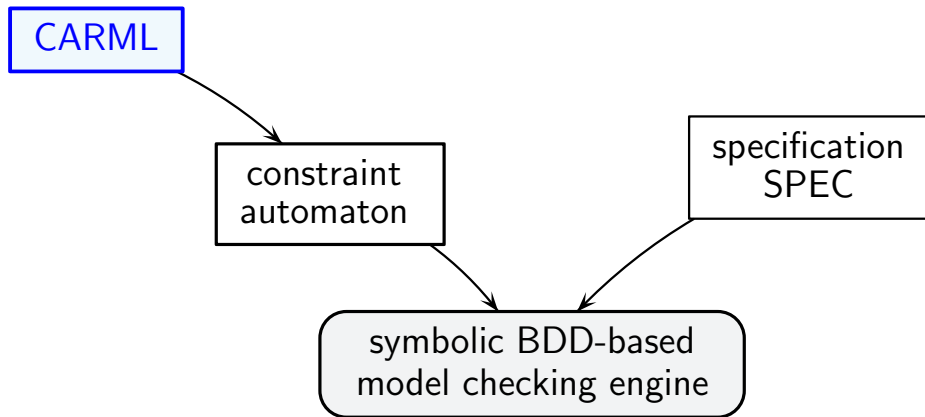


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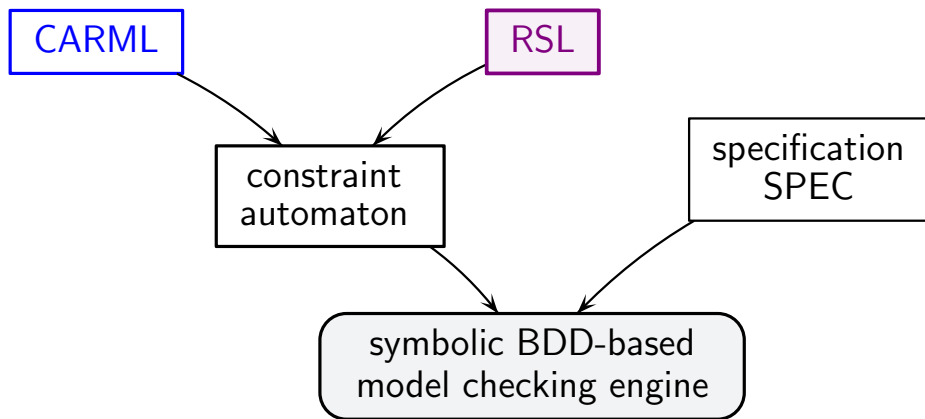
modeling and verification toolset for CA & Reo





relies on a hybrid modeling approach

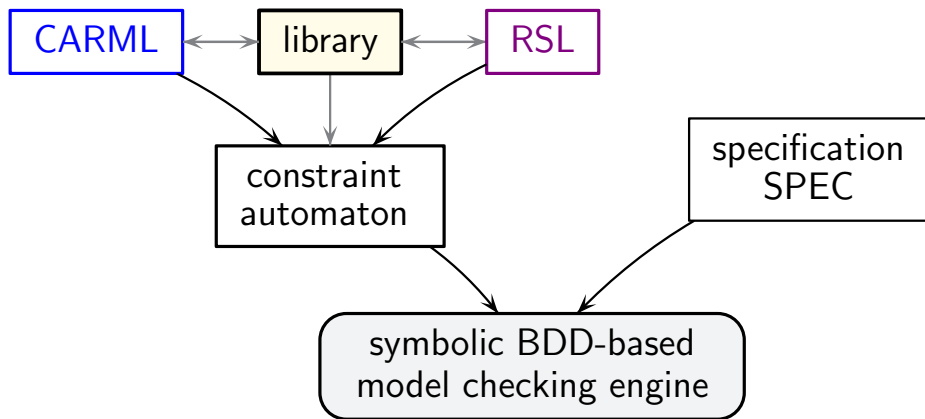
CARML guarded command language for specifying CA
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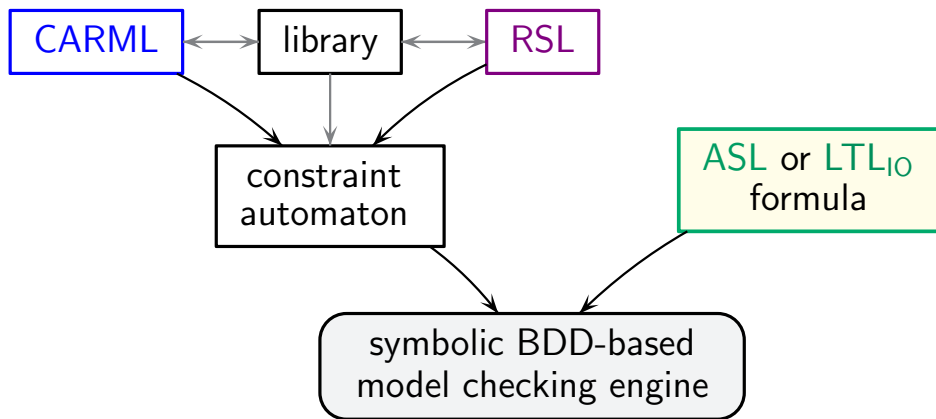
RSL Reo scripting language



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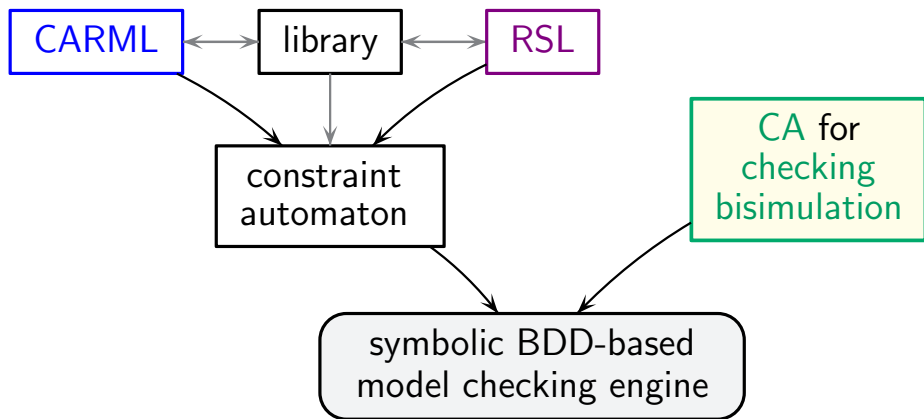
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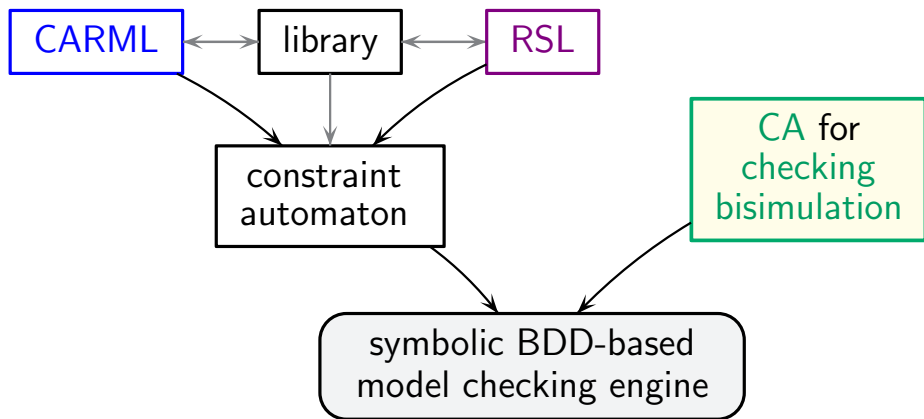
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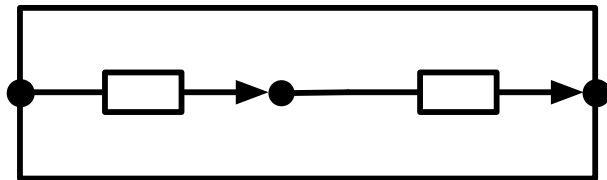
- temporal logics **ASL** and (fragment of) **LTL_{IO}**
- bisimulation checking



integrated in the **Extensible Coordination Tools** GUI
graphical Reo network editor, RSL import/export,
counterexample/witness animations,...

Example: RSL script for FIFO with k buffer cells

970



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CIRCUIT FIFO<k> {  
  for (i=0;i<k;i=i+1) {  
    f[i] = new FIFO1;  
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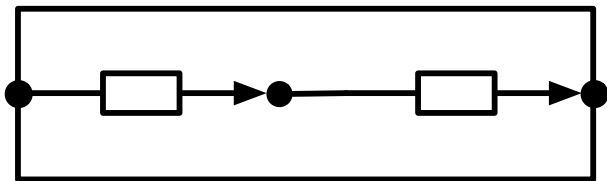


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- component interfaces C_1, \dots, C_n
- glue code \mathcal{R}
- composite system $C_1 \parallel \dots \parallel C_n \parallel \mathcal{R}$

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Reo ... elegant, declarative way to specify connectors

- compositional CA-semantics
- well suited for hierarchical design
- very expressive

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embeddings of various other formalisms into Reo

Petri nets

UML sequence diagrams

CCS-like process calculi

name-passing calculi

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various applications, e.g.,

coordination protocols

web-services

electronic auction protocol

biological systems

sensor networks

⋮

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just mild adaptations of known verification techniques

- temporal logics: linear- and branching-time
- bisimulation equivalence checking
- synthesis, compatibility, alternating-time logics

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- variants of CA to model context-sensitive behaviors and dynamic reconfigurations
- better algorithms for compatibility and compositional connector synthesis
- extensions of ASL and LTL_{IO} (towards ASL^*)
- partial-information game semantics for CA, proper game logic