

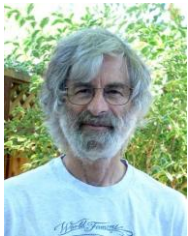
Model Checking of Timed Systems

A UPPAAL Tutorial

Wang Yi
Uppsala University, Sweden
SFM 2010, Bertinoro

1

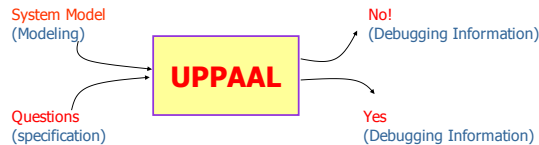
This is simple, simple, simple



LESLIE LAMPORT

2

UPPAAL *A model checker for real-time systems*



Developed by **UPP**sala Univ + **AAL**borg Univ = **UPPAAL**

3

Main Authors/Contributors of UPPAAL

- Johan Bengtsson
- Gerd Behrman
- Alexandre David
- Kim Larsen
- Fredrik Larsson
- Paul Pettersson and
- Wang Yi

OUTLINE

- Model Checking in a Nutshell
- Timed automata and TCTL
- A UPPAAL Tutorial
 - Data structures & central algorithms
 - UPPAAL input languages

(Recent Work: Multi-core Timing Analysis)

5

Main references

- **Temporal Logics (CTL)**
 - Automatic Verification of Finite State Concurrent Systems Using Temporal Logic Specifications: A Practical Approach. Edmund M. Clarke, E. Allen Emerson, A. Prasad Sistla, POPL 1983: 117-126, also as "Automatic Verification of Finite-State Concurrent Systems Using Temporal Logic Specifications. ACM Trans. Program. Lang. Syst. 8(2): 244-263 (1986)"
- **Timed Systems (Timed Automata, TCTL)**
 - A Theory of Timed Automata. Rajeev Alur, David L. Dill. Theor. Comput. Sci. 126(2): 183-235 (1994)
 - Symbolic Model Checking for Real-Time Systems, Thomas A. Henzinger, Xavier Nicollin, Joseph Sifakis, and Sergio Yovine. Information and Computation 111:193-244, 1994.
 - UPPAAL in a Nutshell. Kim Guldstrand Larsen, Paul Pettersson, Wang Yi. STTT 1(1-2): 134-152 (1997)
 - **Timed Automata – Semantics, Algorithms and Tools**, a tutorial on timed automata Johan Bengtsson and Wang Yi: (a book chapter in Rozenberg et al, 2004, LNCS).
 - **On-line help of UPPAAL**: www.uppaal.com

6

Model-Checking

in a Nutshell

7

Merits of model checking ...

- Checking **simple properties** (e.g. deadlock-free) is already extremely useful!
 - It is not to prove that a system is completely correct (bug-free)
- The goal is to have tools that can help a developer **find errors** and **improve the quality** of her/his design.
 - It is to complement testing
- Now widely used in hardware design, protocol design, and hopefully soon, **embedded systems!**

8

History: Model-checking invented in 70's/80s

[Pnueli 77, Clarke et al 83, POPL83, Sifakis et al 82]

- Restrict attention to finite-state systems**
 - Control skeleton + boolean (finite-domain) variables
 - Found in hardware design, communication protocols, process control
- Specification using CTL, LTL etc** [Pnueli, Lamport, Clarke]
 - Safety, Progress/Liveness, Responsiveness etc
- BDD-based symbolic technique** [Bryant 86]
 - SMV 1990 Clarke, McMillan et al, state-space 10^{20}
 - Now powerful tools used in hardware design
- On-the-fly enumerative technique** [Holzman 89]
 - SPIN, COSPAN, CAESAR, KRONOS, IF/BIP, UPPAAL (since 1993) etc
- SAT-based techniques** [Clarke et al ...]

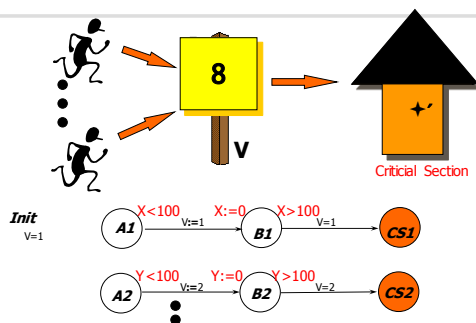
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History: Model checking for real time systems, started in the 80s/90s

- Models of timed systems**
 - Timed automata, [Alur&Dill 1990]
 - Timed process algebras, Timed CSP, Timed CCS [Wang 1990]
- Extension of model checking to consider time quantities**
 - Timed variants of temporal logics e.g TCTL
- Tools**
 - KRONOS, Hytech: 1993 --
 - UPPAAL 1995 --
 - TAB 1993/Prototype of UPPAAL [FORTE94, Wang et al]

10

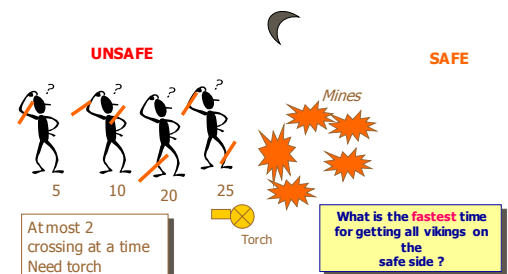
Example: Fischer's Protocol



11

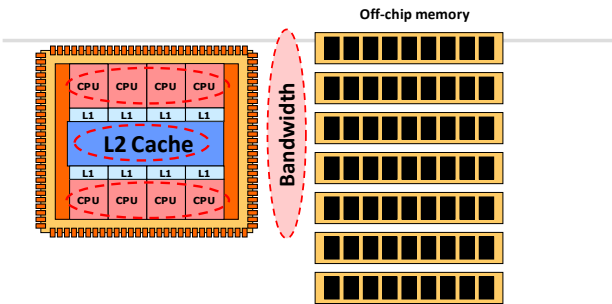
Example: the Vikings Problem

Real time scheduling



12

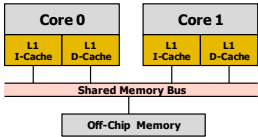
Multicore Challenges



Shared Resources -- cpu's, caches, bandwidth, energy budget etc.

13

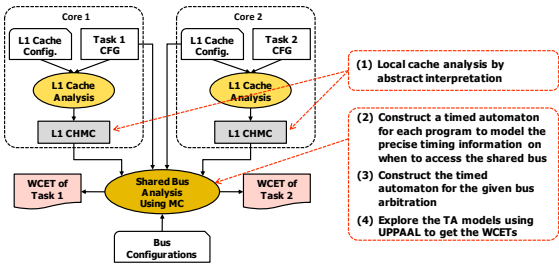
Worst-Case Execution Time Analysis of Concurrent Programs on Multicores



A duo-core processor with private L1 cache and shared memory bus

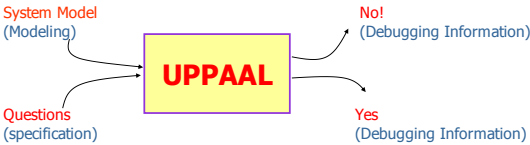
14

Combining Static Analysis & Model-Checking [RTSS 2010, submitted]



15

UPPAAL A model checker for real-time systems

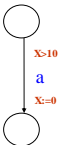


16

MODELING

How to construct Model ?

Modeling Real Time Systems



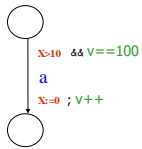
Timed Automaton

- Events
 - synchronization
 - interrupts
- Timing constraints
 - specifying event arrivals
 - e.g. Periodic and sporadic

17

18

Modeling Real Time Systems

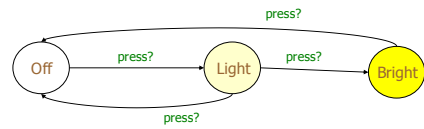


*Timed Automaton
in UPPAAL*

- Events
 - synchronization
 - interrupts
- Timing constraints
 - specifying event arrivals
 - e.g. Periodic and sporadic
- Data variables & C-subset
 - Guards
 - assignments

19

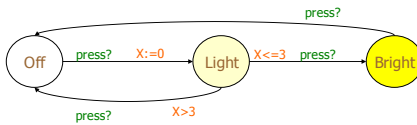
A Light Controller



WANT: if press is issued twice quickly then the light will get brighter; otherwise the light is turned off.

20

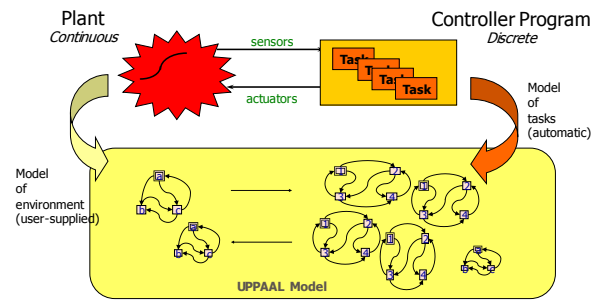
A Light Controller (with timer)



Solution: Add real-valued clock x

21

Construction of Models: Concurrency



22

SPECIFICATION

How to ask questions: Specs ?

23

Specification=Requirement, Lampert 1977

- Safety
 - Something (bad) should not happen
- Liveness
 - Something (good) must happen/should be repeated



24

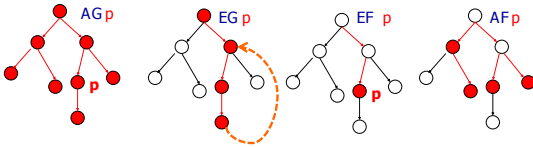
Computation Tree Logic, CTL

Clarke & Emerson 1980

Syntax

$\phi ::= P \mid \neg \phi \mid \phi \vee \phi \mid EX \phi \mid E[\phi U \phi] \mid A[\phi U \phi]$
where $P \in AP$ (atomic propositions)

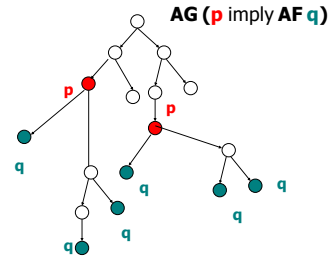
Derived Operators



25

Liveness: $p \rightarrow q$

" p leads to q "



26

Specification: Examples

- Safety**
 - $AG \neg (P1.CS1 \ \& \ P2.CS2)$ **Invariant**
 - $AG (temp > 10 \ \& \ speed < 120)$
 - $EF (time > 60 \rightarrow viking4.safe)$ **Reachability**
 - $EF (viking1.safe \ \& \ viking2.safe \ \& \ viking3.safe \ \& \ viking4.safe)$
- Liveness**
 - $AF (speed > 100)$ **Eventually**
 - $AG (P1.try \rightarrow AF P1.CS1)$ **Leads to**

27

VERIFICATION

Model meets Specs ?

28

Verification

- Semantics of a system**
 - = all states + state transitions
 - (all possible executions)
- Verification**
 - = state space exploration + examination

29

Two basic verification algorithms

- Reachability analysis**
 - Checking safety properties
- Loop detection**
 - Checking liveness properties

30

UPPAAL DEMO

31

OUTLINE

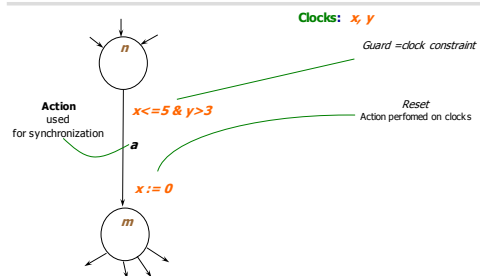
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- (Recent Work: Multicore Timing Analysis)

32

Timed Automata, TCTL & Verification Problems

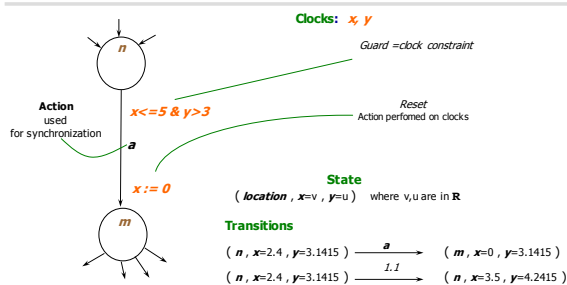
33

Timed Automata: Syntax



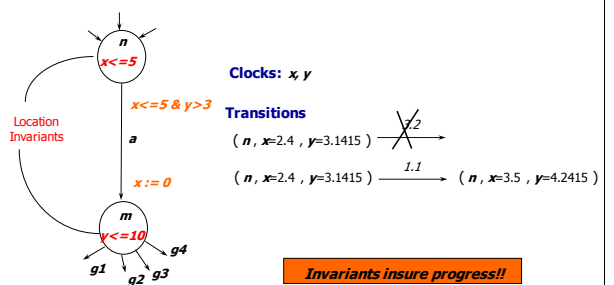
34

Timed Automata: Semantics



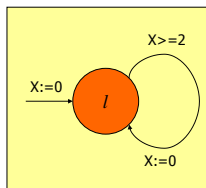
35

Timed Automata with Invariants



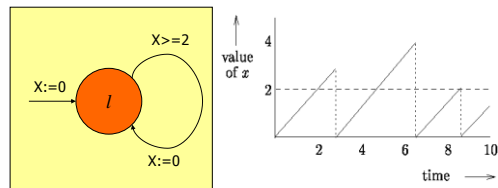
36

Timed Automata: Example



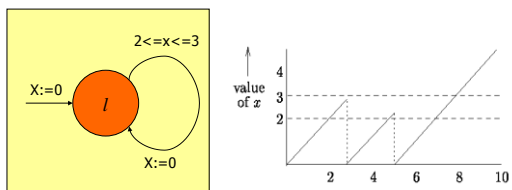
37

Timed Automata: Example



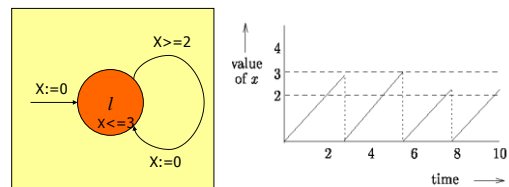
38

Timed Automata: Example



39

Timed Automata: Example



40

Timed Automata

=

Finite Automata + Clock Constraints + Clock resets

41

Clock Constraints

$g ::= x \sim n \mid g \ \& \ g$

where

- x is a clock variable
- $\sim \in \{<, >, \leq, \geq\}$
- n is a natural number and

42

Semantics (definition)

- clock valuations: $V(C) \quad v: C \rightarrow \mathbb{R}_{\geq 0}$
- state: (l, v) where $l \in L$ and $v \in V(C)$
- action transition
 $(l, v) \xrightarrow{a} (l', v') \text{ iff } \textcircled{l} \xrightarrow{g \ a \ r} \textcircled{l'}$
 $g(v) \text{ and } v' = v[r] \text{ and } \text{Inv}(l')(v')$
- delay Transition
 $(l, v) \xrightarrow{d} (l, v+d) \text{ iff}$
 $\text{Inv}(l)(v+d') \text{ whenever } d' \leq d \in \mathbb{R}_{\geq 0}$

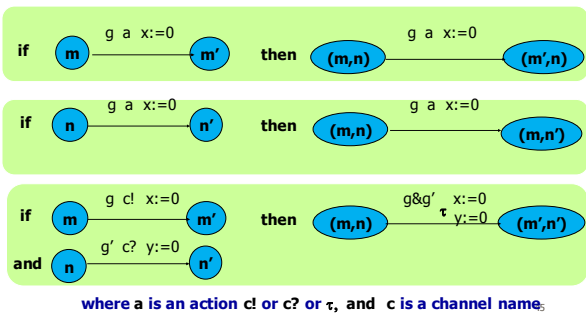
43

Modeling Concurrency

- Products of automata
- CCS Parallel composition
 - implemented in UPPAAL

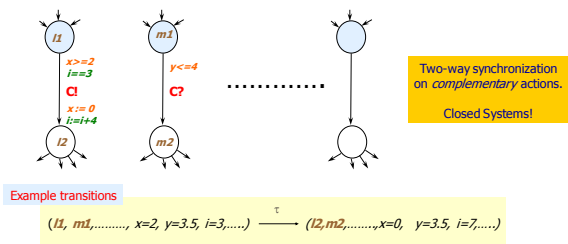
44

CCS Parallel Composition (implemented in UPPAAL)



The UPPAAL Model

= Networks of Timed Automata + Integer Variables +



45

Location Reachability (def.)

n is reachable from m if there is a sequence of transitions:

$$(m, v) \xrightarrow{*} (n, v')$$

47

48

Verification Problems

(Timed) Language Inclusion, $L(A) \subseteq L(B)$

$(a_0, t_0) (a_1, t_1) \dots (a_n, t_n) \in L(A)$

If

"A can perform a_0 at t_0 , a_1 at t_1 ... a_n at t_n "

$(l_0, u_0) \xrightarrow{t_0} (l_0, u_0 + t_0) \xrightarrow{a_0} (l_1, u_1) \dots$

49

Verification Problems

- Timed Language Equivalence & Inclusion ☹
 - 1-clock, finite traces, decidable [Ouaknine & Worrell 04]
 - 1-clock, infinite traces & Buchi-conditions, undecidable [Abdulla et al 05]
- Universality ☹
- Untimed Language Inclusion ☺
- (Un)Timed (Bi)simulation ☺
- Reachability Analysis/Emptiness ☺
- Optimal Reachability (synthesis problem) ☺
 - If a location is reachable, what is the minimal delay before reaching the location?

50

Timed CTL = CTL + clock constraints

Note that the semantics of TA defines a transition system where each state has a **Computation Tree**

51

Computation Tree Logic, CTL

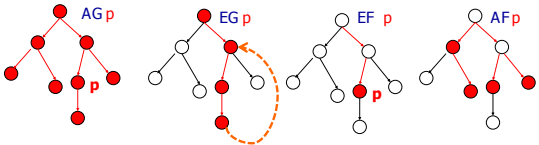
Clarke & Emerson 1980

Syntax

$\phi ::= P \mid \neg \phi \mid \phi \vee \phi \mid EX \phi \mid E[\phi U \phi] \mid A[\phi U \phi]$

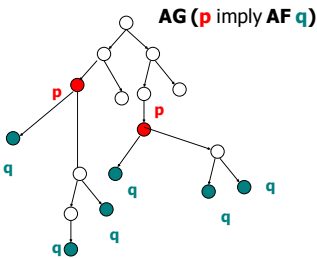
where $P \in AP$ (atomic propositions)

Derived Operators



52

Liveness: $p \rightarrow q$ "p leads to q"



53

Timed CTL (a simplified version)

Syntax

$\phi ::= p \mid \neg \phi \mid \phi \vee \phi \mid EX \phi \mid E[\phi U \phi] \mid A[\phi U \phi]$

where $p \in AP$ (atomic propositions) **OF** Clock constraint

54

Timed CTL (a simplified version)

Syntax

$\phi ::= p \mid \neg \phi \mid \phi \vee \phi \mid EX \phi \mid E[\phi U \phi] \mid A[\phi U \phi]$

where $p \in AP$ (atomic propositions) **OR Clock constraint**

Derived Operators

$AG\ p$

$EG\ p$

$EF\ p$

$AF\ p$

$E<> P$ in UPPAAL

$A<> P$ in UPPAAL

$E[] P$ in UPPAAL

$A<> P$ in UPPAAL

Derived Operators (cont.)

$AG(p \text{ imply } AF\ q)$

$p \dashv\dashv q$ in UPPAAL

56

Bounded Liveness

[TACAS98]

Verify: "whenever p is true, q should be true within 10 sec

$P \dashv\dashv (q \text{ and } x < 10)$

Use extra clock x
Add $x:=0$ on all edges leading to P

57

Bounded Liveness/Responsiveness

[TACAS98]

Verify: "whenever p is true, q should be true within 10 sec

$AG((P_b \text{ and } x > 10) \text{ imply } q)$

Use extra clock x and boolean P_b
Add $P_b := tt$ and $x:=0$ on all edges leading to location P

58

Bounded Liveness/Responsiveness

[TACAS98]

Verify: "whenever p is true, q should be true within 10 sec

$AG((P_b \text{ and } x > 10) \text{ imply } q)$

Use extra clock x and boolean P_b
Add $P_b := tt$ and $x:=0$ on all edges leading to location P

This is not really correct; "not P_b" should be added as guard

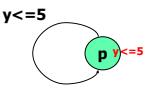
P_b:=ff should be added On all edges leaving q

59

Problem with Zenoness/Time-stop

60

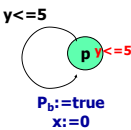
EXAMPLE



We want to specify "whenever P is true, Q should be true within 10 time units"

61

EXAMPLE

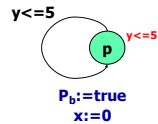


We want to specify "whenever P is true, Q should be true within 10 time units"

AG ((P_b and x > 10) imply Q)

62

EXAMPLE



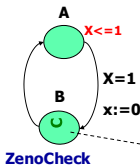
We want to specify "whenever P is true, Q should be true within 10 time units"

AG ((P_b and x > 10) imply q)
is satisfied !!!

63

Solution with UPPAAL

Check Zeno-freeness by an extra observer
System || ZenoCheck



Check (yes means "no zeno loops")
ZenoCheck.A - - > ZenoCheck.B

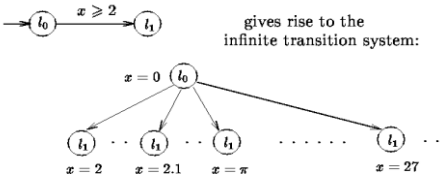
Committed location!

64

REACHABILITY ANALYSIS
using Regions

65

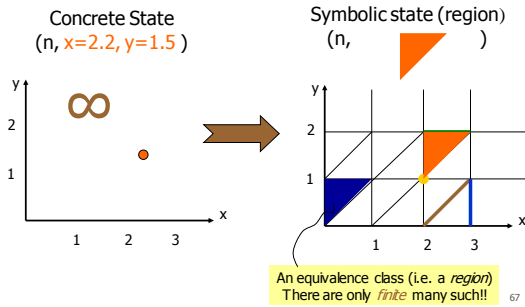
Infinite State Space!



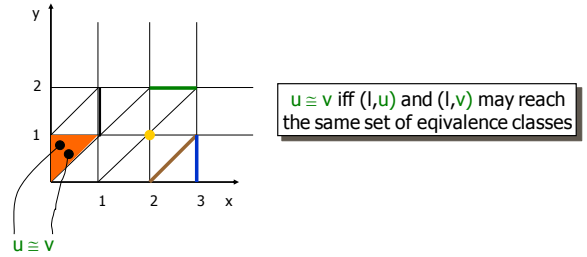
However, the reachability problem is decidable ☺ Alur&Dill 1991

66

Region: From infinite to finite

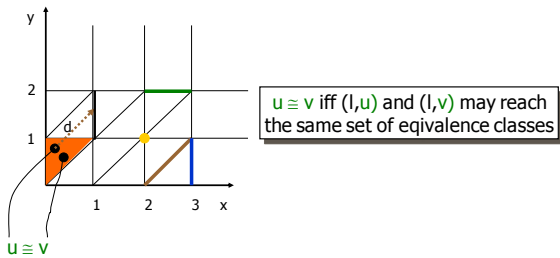


Region equivalence (Intuition)



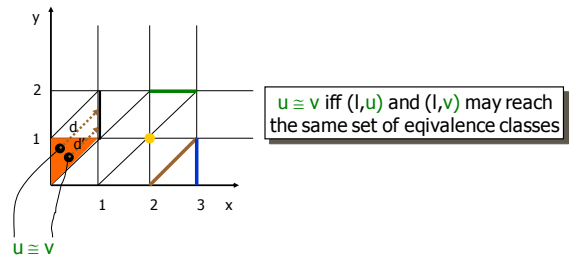
68

Region equivalence (Intuition)



69

Region equivalence (Intuition)



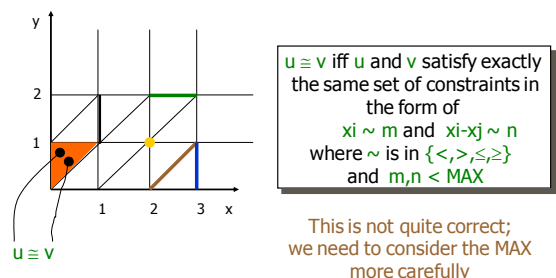
70

Region equivalence [Alur and Dill 1990]

- u, v are clock assignments
- $u \approx v$ iff
 - For all clocks x ,
 - either (1) $u(x) > Cx$ and $v(x) > Cx$
 - or (2) $\lfloor u(x) \rfloor = \lfloor v(x) \rfloor$
 - For all clocks x , if $u(x) \leq Cx$,
 - $\{u(x)\} = 0$ iff $\{v(x)\} = 0$
 - For all clocks x, y , if $u(x) \leq Cx$ and $u(y) \leq Cy$
 - $\{u(x)\} \leq \{u(y)\}$ iff $\{v(x)\} \leq \{v(y)\}$

71

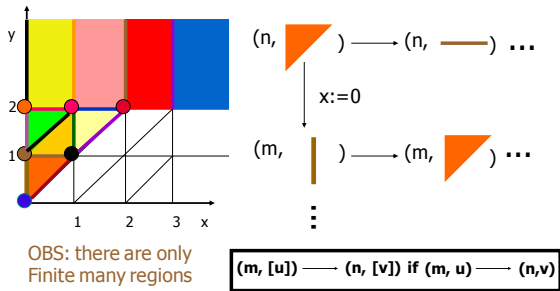
Region equivalence (alternatively)



72

Region Graph

Finite-State Transition System!!



73

Theorem

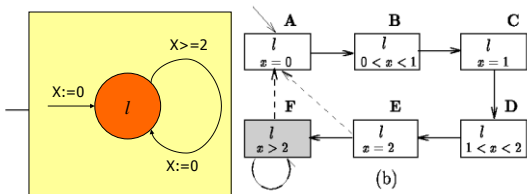
$u \approx v$ implies

- $u(x:=0) \approx v(x:=0)$
- $u+n \approx v+n$ for all natural number n
- for all $d < 1$: $u+d \approx v+d'$ for some $d' < 1$

"Region equivalence" is preserved by "addition" and reset.
(also preserved by "subtraction" if clock values are "bounded")

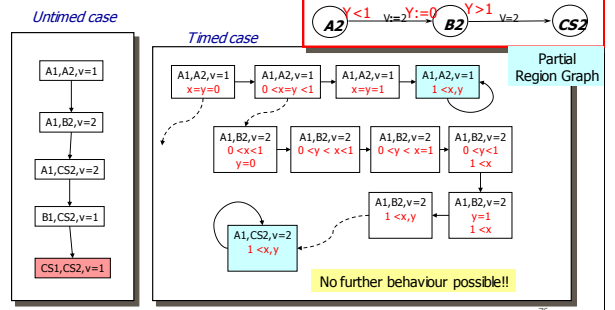
74

Region graph of a simple timed automata



75

Fischers again



76

Problems with Region Construction

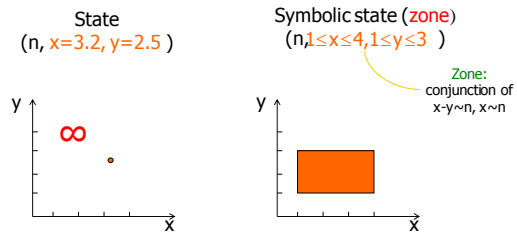
- Too many 'regions'
 - Sensitive to the maximal constants
 - e.g. $x > 1,000,000, y > 1,000,000$ as guards in TA
- The number of regions is highly exponential in the number of clocks and the maximal constants.

77

REACHABILITY ANALYSIS using ZONES

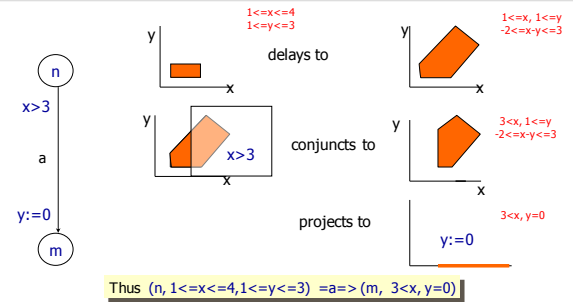
78

Zones: From infinite to finite



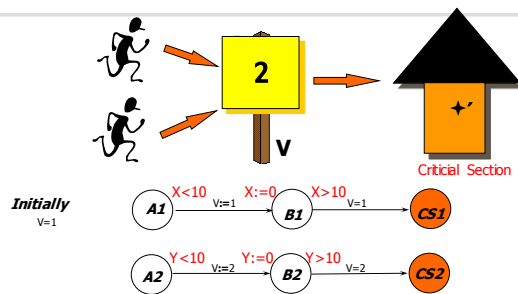
79

Symbolic Transitions



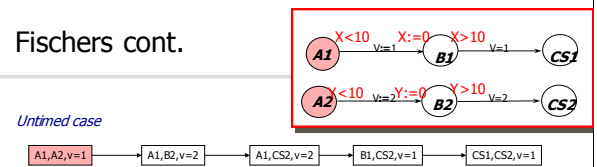
80

Fischer's Protocol analysis using zones



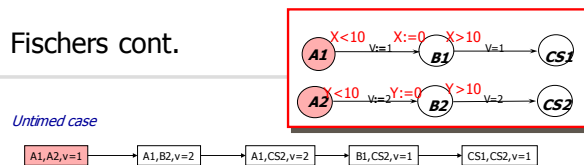
81

Fischers cont.



82

Fischers cont.

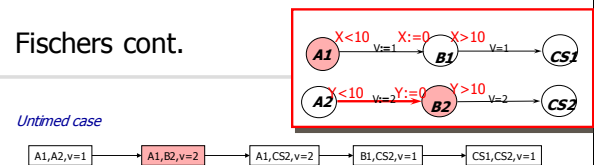


Taking time into account

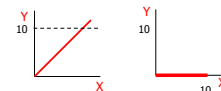


83

Fischers cont.

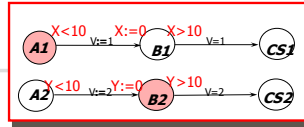


Taking time into account

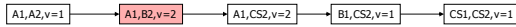


84

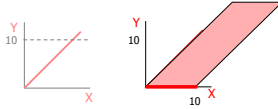
Fischers cont.



Untimed case

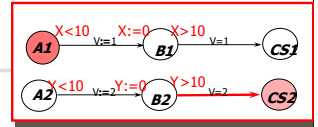


Taking time into account

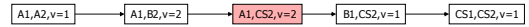


85

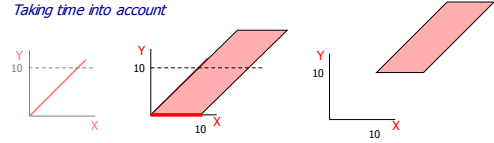
Fischers cont.



Untimed case

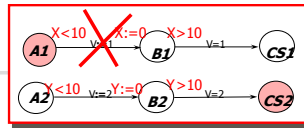


Taking time into account

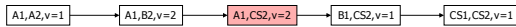


86

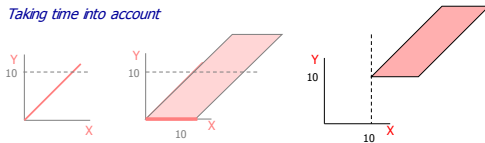
Fischers cont.



Untimed case



Taking time into account



87

Zones = Conjunctive constraints

- A zone Z is a conjunctive formula: $g_1 \ \& \ g_2 \ \& \ \dots \ \& \ g_n$ where g_i may be $x_i \sim b_i$ or $x_i - x_j \sim b_{ij}$
- Use a zero-clock x_0 (constant 0), we have $\{x_i - x_j \sim b_{ij} \mid \sim \text{ is } < \text{ or } \leq, i, j \leq n\}$
- This can be represented as a MATRIX, DBM (Difference Bound Matrices)

88

Solution set as semantics

- Let Z be a zone (a set of constraints)
- Let $[Z] = \{u \mid u \text{ is a solution of } Z\}$

(We shall simply write Z instead $[Z]$)

89

Operations on Zones

- Post-condition (Delay): $SP(Z)$ or Z^\uparrow
 - $[Z^\uparrow] = \{u+d \mid d \in \mathbb{R}, u \in [Z]\}$
- Pre-condition: $WP(Z)$ or Z^\downarrow (the dual of Z^\uparrow)
 - $[Z^\downarrow] = \{u \mid u+d \in [Z] \text{ for some } d \in \mathbb{R}\}$
- Reset: $\{x\}Z$ or $Z(x:=0)$
 - $[\{x\}Z] = \{u[0/x] \mid u \in [Z]\}$
- Conjunction
 - $[Z \& g] = [Z] \cap [g]$

90

Two more operations on Zones

- Inclusion checking: $Z_1 \subseteq Z_2$
 - solution sets
- Emptiness checking: $Z = \emptyset$
 - no solution

91


Theorem on Zones

The set of zones is closed under all zone operations

- That is, the **result** of the operations on a zone is a **zone**
- Thus, there will be a zone to represent the sets: $[Z^\uparrow]$, $[Z^\downarrow]$, $\{\{x\}Z\}$

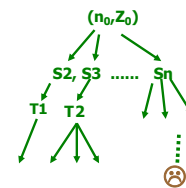
92

One-step reachability: $s_i \rightsquigarrow s_j$

- **Delay:** $(n, Z) \rightarrow (n, Z')$ where $Z' = Z \uparrow \wedge \text{inv}(n)$
- **Action:** $(n, Z) \rightarrow (m, Z')$ where $Z' = \{x\}.Z \wedge g$
 if 
- **Reach:** $(n, Z) \rightsquigarrow (m, Z')$ if $(n, Z) \rightarrow^* (m, Z')$
- **Successors** $(n, Z) = \{(m, Z') \mid (n, Z) \rightsquigarrow (m, Z'), Z' \neq \emptyset\}$

93

Now, we have a search problem



EF 

94

OUTLINE

- Model Checking in a Nutshell
- Timed automata and TCTL
- **A UPPAAL Tutorial**
 - Data structures & central algorithms
 - UPPAAL input languages

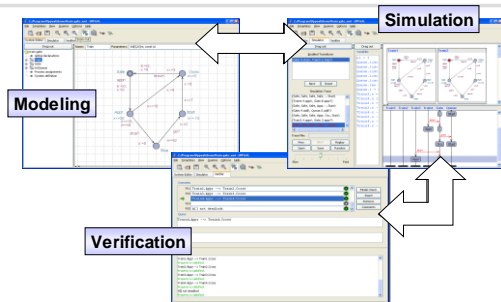
(Recent Work: Multicore Timing Analysis)

95

What's inside UPPAAL

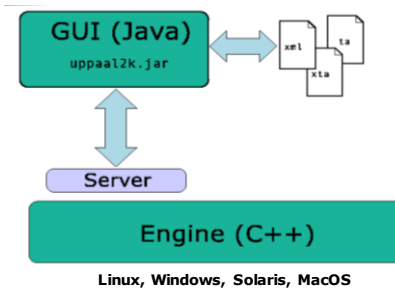
96

UPPAAL Tool



97

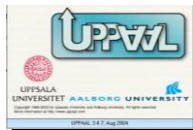
Architecture of UPPAAL



98

Inside the UPPAAL tool

- Data Structures
 - DBM's (Difference Bounds Matrices)
 - Canonical and Minimal Constraints
- Algorithms
 - Reachability analysis
 - Liveness checking
- Verification Options

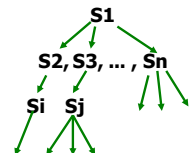


99

All Operations on Zones

(needed for verification)

- Transformation
 - Conjunction
 - Post condition (delay)
 - Reset
- Consistency Checking
 - Inclusion
 - Emptiness



100

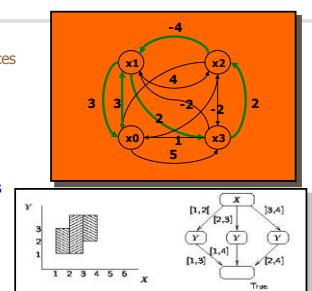
Zones = Conjunctive constraints

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 - where g_i may be $x_i \sim b_i$ or $x_i - x_j \sim b_{ij}$
- Use a zero-clock x_0 (constant 0), we have
 - $\{x_i - x_j \sim b_{ij} \mid \sim \text{is } < \text{ or } \leq, i, j \leq n\}$
- This can be represented as a MATRIX, DBM (Difference Bound Matrices)

101

Datastructures for Zones in UPPAAL

- Difference Bounded Matrices [Bellman58, DB89]
- Minimal Constraint Form [RTSS97]
- Clock Difference Diagrams [CAV99]



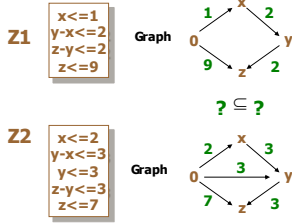
102

Canonical Datastructures for Zones

Difference Bounded Matrices

Bellman 1958, Dill 1989

Inclusion



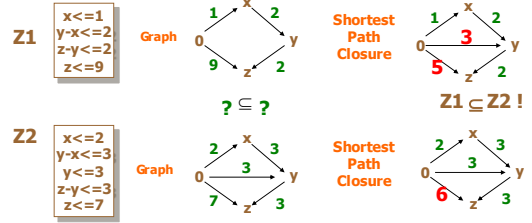
103

Canonical Datastructures for Zones

Difference Bounded Matrices

Bellman 1958, Dill 1989

Inclusion



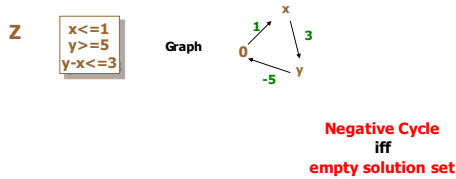
104

Canonical Datastructures for Zones

Difference Bounded Matrices

Bellman 1958, Dill 1989

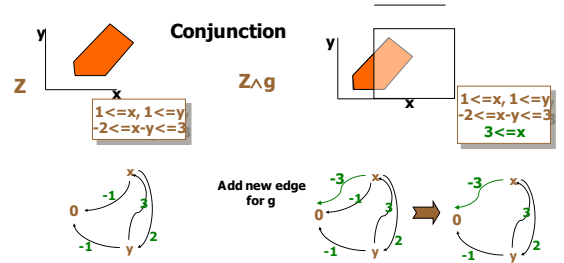
Emptiness



105

Canonical Datastructures for Zones

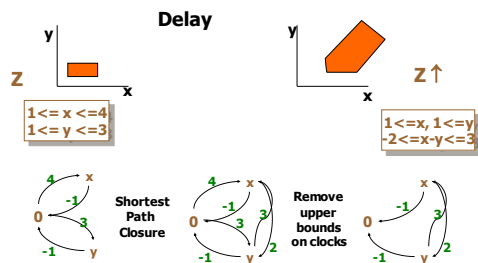
Difference Bounded Matrices



106

Canonical Datastructures for Zones

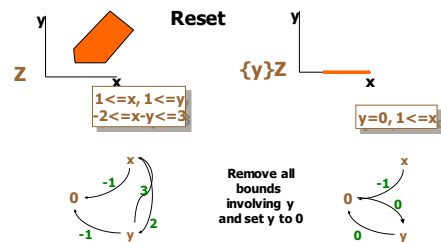
Difference Bounded Matrices



107

Canonical Datastructures for Zones

Difference Bounded Matrices



108

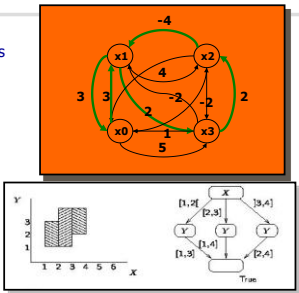
COMPLEXITY

- Computing the shortest path closure, the canonical form of a zone: $O(n^3)$ [Dijkstra's alg.]
- Run-time complexity, mostly in $O(n)$ (when we keep all zones in canonical form)

109

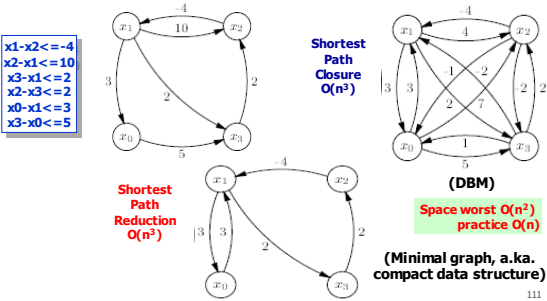
Datastructures for Zones in UPPAAL

- Difference Bounded Matrices [Belman58, Dill89]
- Minimal Constraint Form [RTSS97]
- Clock Difference Diagrams [CAV99]



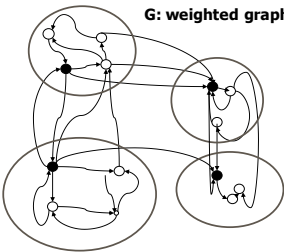
110

Minimal Graph



111

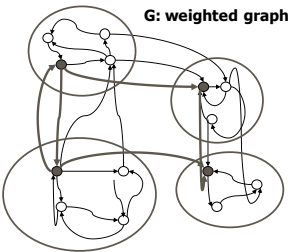
Graph Reduction Algorithm



- Equivalence classes based on 0-cycles.

112

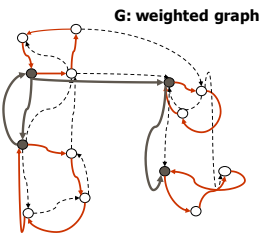
Graph Reduction Algorithm



- Equivalence classes based on 0-cycles.
- Graph based on representatives. Safe to remove redundant edges

113

Graph Reduction Algorithm

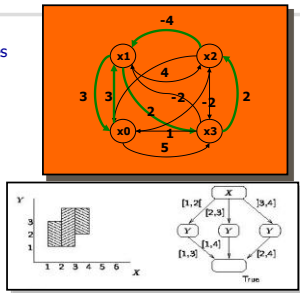


- Equivalence classes based on 0-cycles.
- Graph based on representatives. Safe to remove redundant edges
- Shortest Path Reduction = One cycle pr. class + Removal of redundant edges between classes

114

Datastructures for Zones in UPPAAL

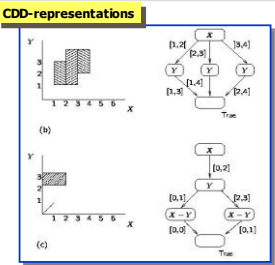
- Difference Bounded Matrices [Bellman58, Dill89]
- Minimal Constraint Form [RTSS97]
- Clock Difference Diagrams [CAV99]



115

Other Symbolic Datastructures

- NDD's Maler et. al.
- CDD's UPPAAL/CAV99
- DDD's Möller, Lichtenberg
- Polyhedra HyTech
-



116

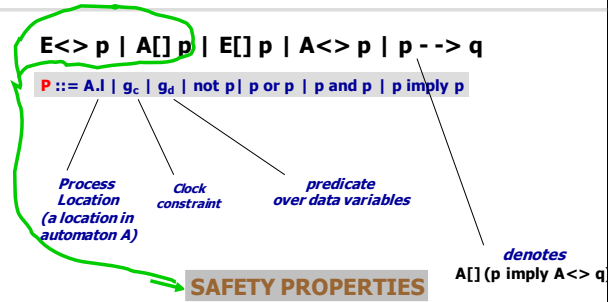
Inside the UPPAAL tool

- Data Structures
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- Algorithms
 - Reachability analysis
 - Liveness checking
- Verification Options



117

Timed CTL in UPPAAL



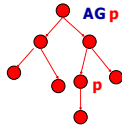
118

Timed CTL (a simplified version)

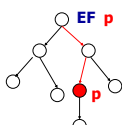
Syntax

$\phi ::= p \mid \neg \phi \mid \phi \vee \phi \mid \text{EX } \phi \mid \text{E}[\phi \text{ U } \phi] \mid \text{A}[\phi \text{ U } \phi]$
where $p \in \text{AP}$ (atomic propositions) OR Clock constraint

Derived Operators

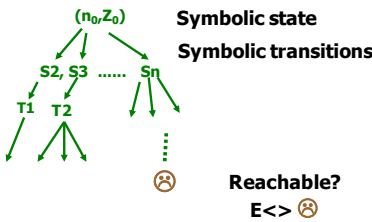


$E<> p$ in UPPAAL



$E[] p$ in UPPAAL

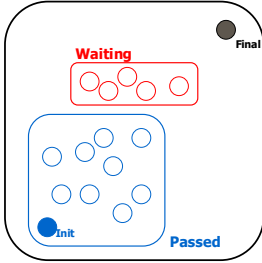
We have a search problem



120

Forward Reachability

Init -> Final ?



```
INITIAL Passed := ∅;
Waiting := {(n0,Z0)};

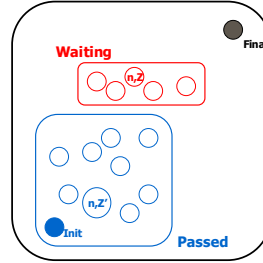
REPEAT
- pick (n,Z) in Waiting
- if for some Z' Z
(n,Z') in Passed then STOP
- else /explore/ add
{(m,U) : (n,Z) => (m,U)}
to Waiting;
Add (n,Z) to Passed

UNTIL Waiting = ∅
or
Final is in Waiting
```

121

Forward Reachability

Init -> Final ?



```
INITIAL Passed := ∅;
Waiting := {(n0,Z0)};

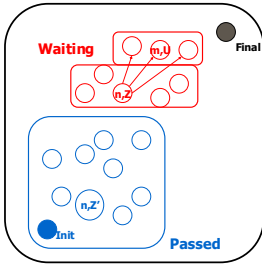
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122

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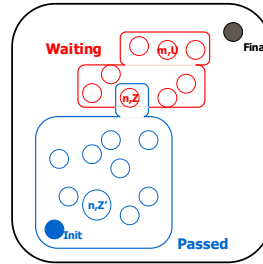
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123

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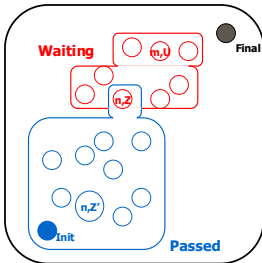
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Add (n,Z) to Passed

UNTIL Waiting = ∅
or
Final is in Waiting
```

124

Forward Reachability

Init -> Final ?



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INITIAL Passed := ∅;
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REPEAT
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- if for some Z' Z
(n,Z') in Passed then STOP
- else /explore/ add
{(m,U) : (n,Z) => (m,U)}
to Waiting;
Add (n,Z) to Passed

UNTIL Waiting = ∅
or
Final is in Waiting
```

125

Further question

Can we find the path with **shortest delay**, leading to P ?
(i.e. a state satisfying P)

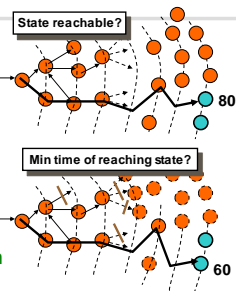
OBSERVATION:

Many scheduling problems can be phrased naturally as reachability problems for timed automata.

126

Verification vs. Optimization

- Verification Algorithms:**
 - Checks a logical property of the entire state-space of a model.
 - Efficient Blind search.
- Optimization Algorithms:**
 - Finds (near) optimal solutions.
 - Uses techniques to avoid non-optimal parts of the state-space (e.g. Branch and Bound).
- Goal:** solve opt. problems with verification.



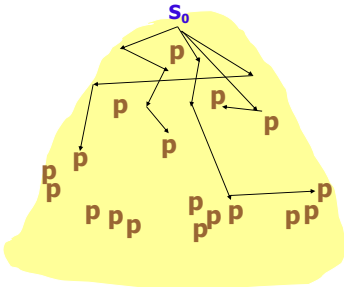
127

OPTIMAL REACHABILITY

The maximal and minimal delay problem

128

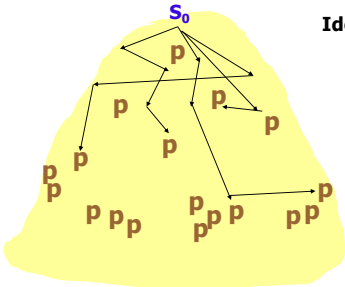
Find the trace leading to P with min delay



There may be a lot of paths leading to P
Which one with the shortest delay?

129

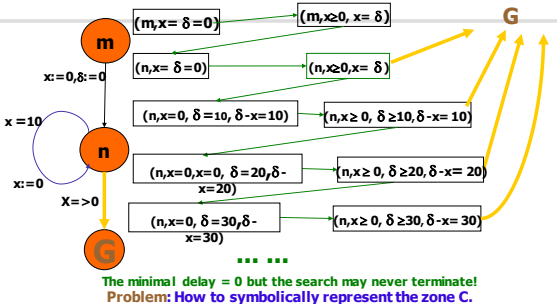
Find the trace leading to P with min delay



Idea: delay as "Cost" to reach a state, thus cost increases with time at rate 1

130

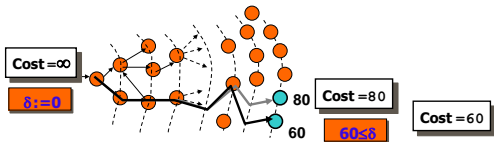
Example (min delay to reach G)



131

An Simple Algorithm for minimal-cost reachability

- State-Space Exploration + Use of global variable Cost and global clock δ
- Update Cost whenever goal state with $\min(C) < Cost$ is found:



- Terminates when entire state-space is explored.
- Problem: The search may never terminate!

132

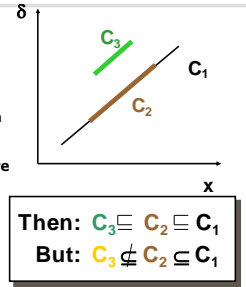
Priced-Zone

- Cost = minimal total time
- C can be represented as the zone Z^δ , where:
 - Z^δ original (ordinary) DBM plus...
 - δ clock keeping track of the cost/time.
- Delay, Reset, Conjunction etc. on Z are the standard DBM-operations
- Delay-Cost is incremented by Delay-operation on Z^δ .

133

Priced-Zone

- Cost = min total time
- C can be represented as the zone Z^δ , where:
 - Z^δ is the original zone Z extended with the global clock δ keeping track of the cost/time.
 - Delay, Reset, Conjunction etc. on C are the standard DBM-operations
- But inclusion-checking will be different



134

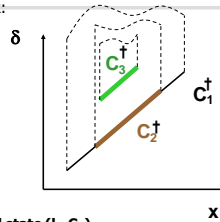
Solution: $()^+$ -widening operation

- $()^+$ removes upper bound on the δ -clock:

$$C_3 \subseteq C_2 \subseteq C_1$$

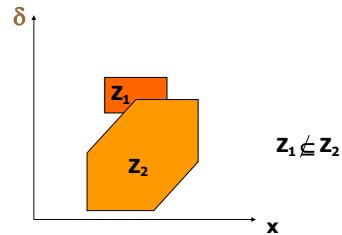
$$C_3^+ \subseteq C_2^+ \subseteq C_1^+$$

- In the Algorithm:
 - $\text{Delay}(C^+) = (\text{Delay}(C))^+$
 - $\text{Reset}(x, C^+) = (\text{Reset}(x, C))^+$
 - $C_1^+ \wedge g = (C_1^+ \wedge g)^+$
- It suffices to apply $()^+$ to the initial state (I_0, C_0) .



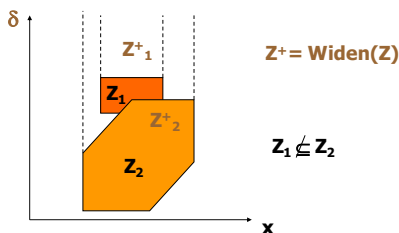
135

Example (widening for Min)



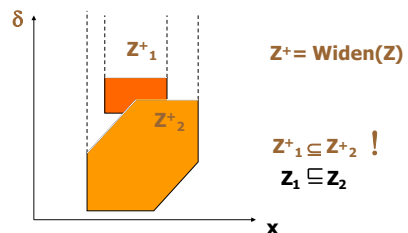
136

Example (widening for Min)



137

Example (widening for Min)



138

An Algorithm (Min)

```

Cost := ∞, Pass := {}, Wait := {(l0, C0)}
while Wait ≠ {} do
  select (l, C) from Wait
  if (l, C) ⊨ P and Min(C) < Cost then Cost := Min(C)
  if (l, C) ⊆ (l, C') for some (l, C') in Pass then skip
  otherwise add (l, C) to Pass
  and forall (m, C') such that (l, C) → (m, C') :
    add (m, C') to Wait
Return Cost

```

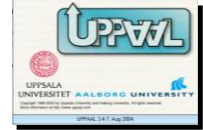
One-step reachability relation

Output: Cost = the min cost of a found trace satisfying P .

139

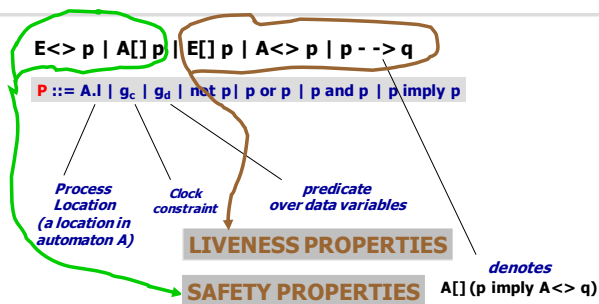
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140

Timed CTL in UPPAAL



141

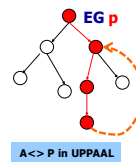
Timed CTL (a simplified version)

Syntax

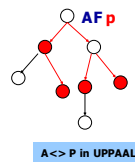
$\phi ::= p \mid \neg \phi \mid \phi \vee \phi \mid EX \phi \mid E[\phi U \phi] \mid A[\phi U \phi]$

where $p \in AP$ (atomic propositions) OR Clock constraint

Derived Operators

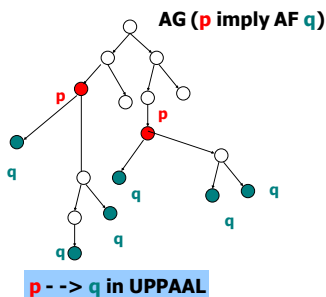


142



143

Derived Operators (cont.)

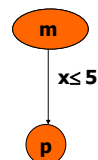


143

Question

$A \langle \rangle p$

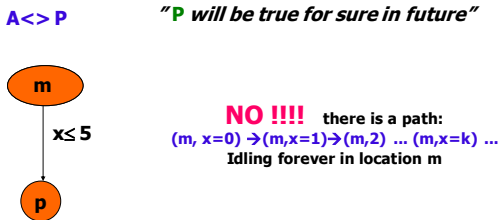
"p will be true for sure in future"



?? Does this automaton satisfy $AF p$

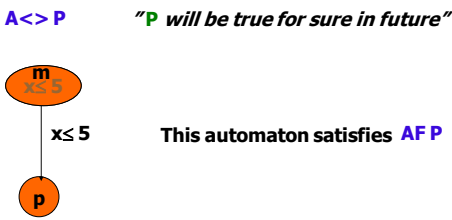
144

Note that



145

Note that



146

Question: Time bound synthesis

Algorithm for checking $A \langle \rangle P$ Eventually P

Bouajjani, Tripakis, Yovine'97
On-the-fly symbolic model checking of TCTL

There is no cycle containing
only states where p is false

147

$A \langle \rangle P$ "P will be true eventually"
But no time bound is given.

Assume **AF P** is satisfied by an automaton A.
Can we calculate the **Max** time bound?

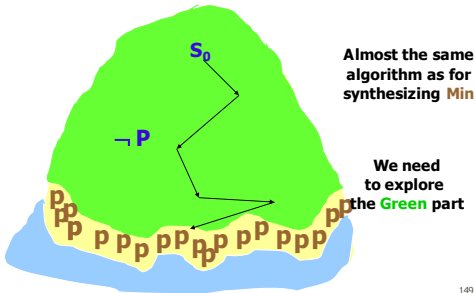
OBS: we know how to calculate the **Min** !

148

not available in the distributed version of UPPAAL

Assume $A \langle \rangle P$ is satisfied

Find the trace leading to P with the **max** delay



149

An Algorithm (Max)

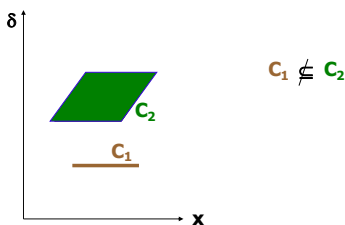
```
Cost:=0, Pass := {}, Wait := {(l0, C0)}  
while Wait ≠ {} do  
  select (l, C) from Wait  
  if (l, C) ⊨ P and Max(C) > Cost then Cost := Max(C)  
  else if forall (l, C') in Pass: C ⊈ C' then  
    add (l, C) to Pass  
    forall (m, C') such that (l, C) → (m, C') :  
      add (m, C') to Wait  
Return Cost
```

One-step reachability relation

Output: Cost = the max cost of a found trace satisfying P.
BUT: \sqsubseteq is defined on zones where the lower bound of "cost" is removed

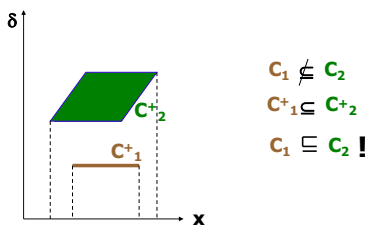
150

Zone-Widening operation for Max



151

Zone-Widening operation for Max



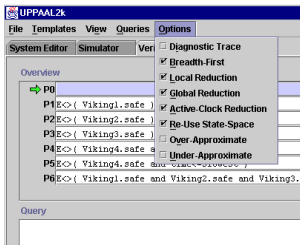
152

Inside the UPPAAL tool

- Data Structures
 - DBM's (Difference Bounds Matrices)
 - Canonical and Minimal Constraints
 - Algorithms
 - Reachability analysis
 - Liveness checking
- ➔ Verification Options



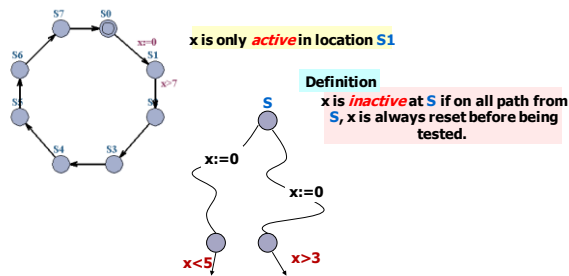
153



- Diagnostic Trace
 - Breadth-First
 - Depth-First
- Local Reduction
- Active-Clock Reduction
- Global Reduction
- Re-Use State-Space
- Over-Approximation
- Under-Approximation

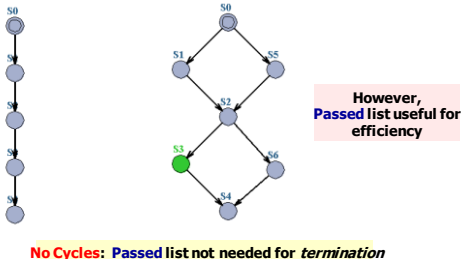
154

Inactive (passive) Clock Reduction



155

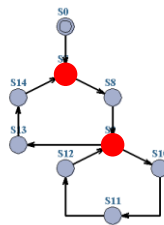
Global Reduction
(When to store symbolic state)



156

Global Reduction

(When to store symbolic state) [RTSS97]

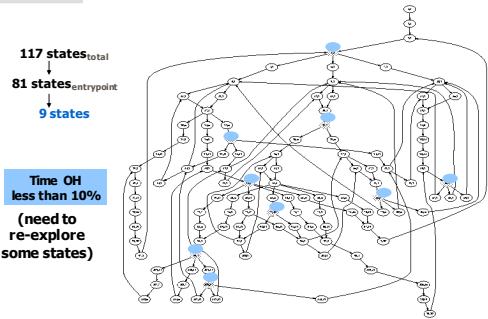


Cycles:
Only symbolic states
involving loop-entry points
need to be saved on **Passed** list

157

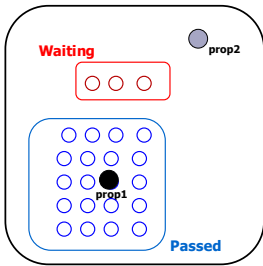
To Store Or Not To Store?

[RTSS97,CAV03]



38

Reuse of State Space



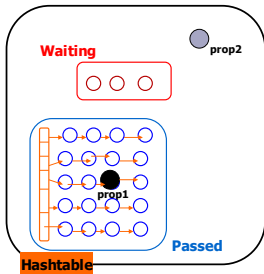
A[] prop1
A[] prop2
A[] prop3
A[] prop4
A[] prop5
.
.
A[] propn

Search in existing Passed list before continuing search

Which order to search?

159

Reuse of State Space



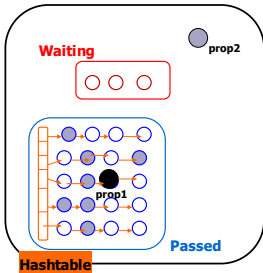
A[] prop1
A[] prop2
A[] prop3
A[] prop4
A[] prop5
.
.
A[] propn

Search in existing Passed list before continuing search

Which order to search?

160

Reuse of State Space



A[] prop1
A[] prop2
A[] prop3
A[] prop4
A[] prop5
.
.
A[] propn

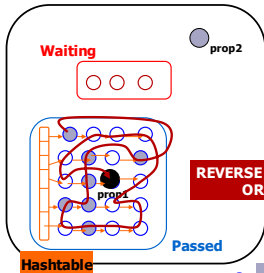
Search in existing Passed list before continuing search

Which order to search?

Swapped to secondary memory

161

Reuse of State Space



A[] prop1
A[] prop2
A[] prop3
A[] prop4
A[] prop5
.
.
A[] propn

Search in existing Passed list before continuing search

Which order to search?

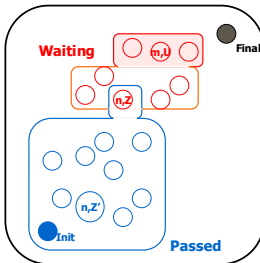
REVERSE CREATION ORDER

generation order

Swapped to secondary memory

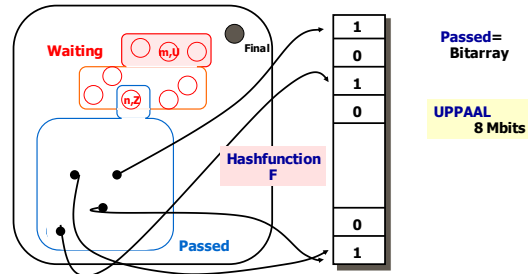
162

Under-approximation *Bitstate Hashing* (Holzman,SPIN)



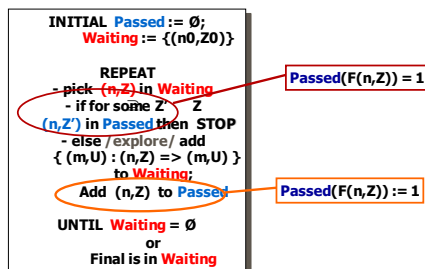
163

Under-approximation *Bitstate Hashing*



164

Bit-state Hashing



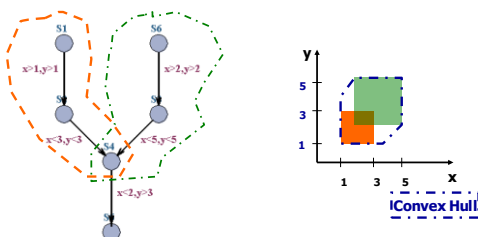
165

Under Approximation (good for finding Bugs quickly, debugging)

- Positive answer is safe (you can trust)
 - You can trust your tool if it tells: a state is reachable (it means Reachable!)
- Negative answer is Inconclusive
 - You should not trust your tool if it tells: a state is non-reachable
 - Some of the branch may be terminated by conflict (the same hashing value of two states)

166

Over-approximation *Convex Hull*



167

Over-Approximation (good for safety property-checking)

- Positive answer is Inconclusive
 - a state is reachable means Nothing (you should not trust your tool when it says so)
 - Some of the transitions may be enabled by Enlarged zones
- Negative answer is safe
 - a state is not reachable means Non-reachable (you can trust your tool when it says so)

168

Now, you can go home

- Download and use UPPAAL or
- Start to implement your own model checker